NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

THESIS

DEVELOPMENT OF THREE-PHASE SOURCE INVERTER FOR RESEARCH AND LABORATORIES

by

Henry O. Amadasu

March 2011

Thesis Advisor: Alexander L. Julian
Second Reader: Roberto Cristi

Approved for public release; distribution is unlimited

THIS PAGE INTENTIONALLY LEFT BLANK

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.			
1. AGENCY USE ONLY ***(Leave blank)***	**2. REPORT DATE** March 2011	**3. REPORT TYPE AND DATES COVERED** Master's Thesis	
4. TITLE AND SUBTITLE Development of Three-Phase Source Inverter for Research and Laboratories		**5. FUNDING NUMBERS**	
6. AUTHOR(S) Henry O. Amadasu			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey, CA 93943-5000		**8. PERFORMING ORGANIZATION REPORT NUMBER**	
9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES) N/A		**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**	
11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government. IRB Protocol Number_____N/A_____.			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution is unlimited		**12b. DISTRIBUTION CODE**	
13. ABSTRACT (maximum 200 words) The small-scale implementation of a power system that explores a three-phase voltage source inverter (VSI) controlled by a Field Programmable Gate Array (FPGA) is investigated in this thesis. The Naval Postgraduate School (NPS) continuously develops new power systems that explore FPGA control of power electronics. The development, testing and documentation of a three-phase voltage source inverter interfacing with an FPGA and hardware is focused on in this thesis. The development of a three-phase VSI, the thermal and power loss analysis of a three-phase VSI and the hardware interface between the FPGA and the three-phase VSI used for research and laboratory procedures at NPS are particularly concentrated on.			
14. SUBJECT TERMS Three-Phase Source Inverter, Field Programmable Gate Array (FPGA), Circuit Board Design and Thermal Behavior Analysis			**15. NUMBER OF PAGES** 85
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	**18. SECURITY CLASSIFICATION OF THIS PAGE** Unclassified	**19. SECURITY CLASSIFICATION OF ABSTRACT** Unclassified	**20. LIMITATION OF ABSTRACT** UU

NSN 7540-01-280-5500 Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

THIS PAGE LEFT INTENTIONALLY BLANK

Approved for public release; distribution is unlimited

DEVELOPMENT OF THREE-PHASE SOURCE INVERTER FOR RESEARCH AND LABORATORIES

Henry O. Amadasu
Lieutenant, United States Navy
B.S., Norfolk State University, 2002

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 2011

Author: Henry O. Amadasu

Approved by: Alexander L. Julian
Thesis Advisor

Roberto Cristi
Second Reader

R. Clark Robertson
Chairman, Department of Electrical and
Computer Engineering

THIS PAGE INTENTIONALLY LEFT BLANK

ABSTRACT

The small-scale implementation of a power system that explores a three-phase voltage source inverter (VSI) controlled by a Field Programmable Gate Array (FPGA) is investigated in this thesis. The Naval Postgraduate School (NPS) continuously develops new power systems that explore FPGA control of power electronics. The development, testing and documentation of a three-phase voltage source inverter interfacing with an FPGA and hardware is focused on in this thesis. The development of a three-phase VSI, the thermal and power loss analysis of a three-phase VSI and the hardware interface between the FPGA and the three-phase VSI used for research and laboratory procedures at NPS are particularly concentrated on.

THIS PAGE INTENTIONALLY LEFT BLANK

TABLE OF CONTENTS

THIS PAGE INTENTIONALLY LEFT BLANK

LIST OF FIGURES

THIS PAGE INTENTIONALLY LEFT BLANK

LIST OF TABLES

THIS PAGE INTENTIONALLY LEFT BLANK

LIST OF ACRONYMS AND ABBREVIATIONS

A	Amps
A/D	Analog to Digital Converter
ac	Alternating Current
C/W	Degree per Watt
COTS	Commercial off the Self
D/A	Digital to Analog Converter
dB	Decibel
dc	Direct Current
dc-ac	Direct Current to Alternating Current
EMI	Electromagnetic Interference
ESO	Electric Ships Office
FPD	Field Programmable Device
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
IPS	Integrated Power Systems
LC	Inductance Capacitive
MOSFET	Metal-Oxide-Silicon Field Effect Transistor
NAVSEA	Naval Sea Systems Command
NGIPS	Next Generation Integrated Power Systems
NPS	Naval Post Graduate School
ns	Nanosecond
PCB	Printed Circuit Board
PETS	Power Electronics Teaching System
PWM	Pulse Width Modulation
R	Resistance
R&D	Research and Development
RMS	Root Mean Square

SDC	Student Design Center
THD	Total Harmonic Distortion
V	Volts
VSI	Voltage Source Inverter
W	WATTS
Z	Impedance
ZEDS	Zonal Electrical Distribution System

ACKNOWLEDGMENTS

I would like to express my sincere appreciation to my thesis advisor Professor Julian for his patience, encouragement and guidance on my education and support through the completion of my thesis. Thanks to the faculty and staff of the Naval Postgraduate School for your dedication to the ideals of higher education.

Special thanks to Nick Hoffman, Stamatios Orfanos-Pepainas and also laboratory technicians Jeff Knight and Warren Rogers who were always ready and willing to assist.

Most importantly, thanks to my very special friend Kaytie Tong, my beautiful children and my parents for all their support and encouragement.

THIS PAGE INTENTIONALLY LEFT BLANK

EXECUTIVE SUMMARY

Future Navy ships will benefit from more compact, integrated, lighter and more versatile power electronics. The existing direct current (dc) Zonal Electrical Distribution System (ZEDS) requires a more innovative approach to the conversion of dc power to alternating current (ac) for motor drives. These innovations could save cost, improve efficiency and enhance the overall war fighting capability of future ships.

Today, COTS (Commercial off the Self) technology is of great interest for military applications. The Secretary of the Navy has stated that the electric drive would be used to propel all future Navy Ships. As a result, the Navy has initiated the Next Generation Integrated Power Systems (NGIPS) effort with centralized leadership by the Electric Ships Office (ESO). The mission of the ESO (PMS 320, organizationally a part of the Program Executive Office—Ships) is to develop and provide smaller, simpler, more affordable, and more capable ship power systems for all Navy platforms by defining open architectures, developing common components, and focusing Navy and industry investments.

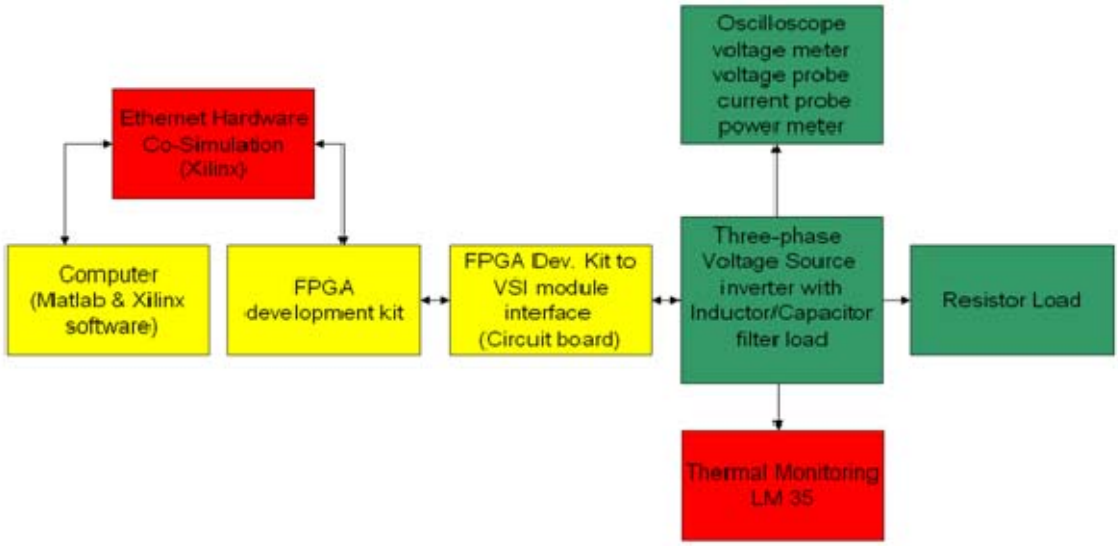
The newly developed voltage source inverter (VSI) encompasses this vision by selecting the insulated gate bipolar transistor (IGBT) Intelligent Power Module (IPM) as its choice for a high performance, optimum cost, optimum volume and increased system reliability device. The IGBT IPM key features include a 17A, 600V, three-phase IGBT inverter bridge including gate driving control integrated

circuit (IC) and freewheeling diodes, short circuit protected IGBT's, a thermal monitoring surface mount, smart shutdown and a comparator fault detection function. This thesis focused on the interface between a Field Programmable Gate Array (FPGA) and the VSI. Emphasis was placed on the design, layout, and testing of the interface, as well as techniques used to minimize or eliminate adverse performance due to electromagnetic interference (EMI).

The development of the three-phase VSI on a printed circuit board for research at NPS was proposed to downscale the current Semikron-Semiteach Power Electronics Teaching System (PETS) module to an integrated, cost optimized, size optimized, and readily available solution. The Student Design Center (SDC) at NPS was created to expose students to the process of transforming performance requirements into power electronics design. The three-phase VSI was incorporated into the design center exercises and student design concepts using software simulation and actual hardware to verify laboratory results.

This thesis begins with a brief introduction to the new VSI, the theory of operation of the IGBT IPM, its purpose, motivation, and research goals. Similarly, the design, layout, thermal analysis, and hardware interfaces, such as the FPGA and Chipscope, are discussed to provide the reader with a better understanding of the software associated with the simulation and testing process. Overall, the new Laboratory VSI achieves a small-scale, less costly implementation of a power system, as well as providing an avenue for establishing a more flexible

research and testing capability here at NPS. The hardware interfaces of the proposed VSI configuration are depicted in the following figure.



VSI Hardware Configuration.

THIS PAGE INTENTIONALLY LEFT BLANK

I. INTRODUCTION

A. PURPOSE

The development of the three-phase voltage source inverter (VSI) on a printed circuit board for research at NPS was proposed to downscale the current Semikron Semiteach power electronics teaching system (PETS) to a more integrated, cost optimized, and size optimized solution. The insulated gate bipolar transistor (IGBT) based pulse width modulated (PWM) VSI was selected as the inverter of choice for ac-fed motor drives. The power stage, which mainly consists of the rectifier, bridge inverter IGBT, thermal management system, inductive-capacitive (LC) filter load and a resistive load, is the major contributor to VSI overall cost and size. The work in this thesis was developed to expose students to the process of transforming performance requirements into a power electronics design. The three-phase VSI incorporated into the Student Design Center (SDC) exercises the student's design concepts using a newly released three-phase IGBT inverter bridge, software simulation, and hardware to verify results. Laboratory sessions using the SDC provide students with flexible procedures and testing capability to conduct research in a real-world environment while preparing them for future study in power electronics design and control [1].

B. MOTIVATION

Future Navy ships will require a more compact, integrated, lighter and more versatile power electronics system. The Naval Sea Systems Command (NAVSEA) is

interested in white papers for long and short-term research and development (R&D) projects that offer potential for advancement and improvements in the implementation of shipboard Integrated Power Systems (IPS) at the major component, subsystem and system level [2]. As a result, the current dc Zonal Electrical Distribution System (ZEDS) requires a more innovative approach to the conversion of dc power to ac power for motor drives. These innovations could save cost, improve the efficiency and enhance the overall war fighting capability of future ships. The newly developed VSI encompasses this vision by using the IGBT IPM as its main part. The IGBT IPM provides a compact, high performance ac motor drive for a simple and optimum layout for reduced component and cost savings [3]. A field programmable gate array (FPGA) controls an IGBT IPM easily with high reliability and frequency.

The IGBT IPM key features comprise a 17A, 600V, three-phase IGBT inverter bridge including gate driving control integrated circuit (IC) and freewheeling diodes, short circuit protected IGBT’s, a thermal monitoring surface mount, smart shutdown and a comparator fault detection function [3]. The exploration of the interface between an FPGA and voltage source inverter (VSI) were focused on in this thesis. Emphasis is placed on the design, layout, and testing of the interface, as well as thermal performance.

A secondary objective is to present the reader with an experimental result based on thermal analysis of the IGBT IPM device and an overview of the VSI hardware and software used in the student design center (SDC) and current FPGA technology.

C. APPROACH

The three-phase VSI printed circuit board (PCB) consists of an IGBT IPM employing three parallel-connected half-bridges, three gate signals and an optional temperature monitoring surface mount. The three-phase inverter is connected to an LC filter in a delta configuration to run a load of three variable resistors in delta configuration. The PCB consists of two current sensors, three voltage sensors, and multiple optocouplers for ground isolation. The PCB's were designed and constructed to interface the FPGA with a Virtex-4 development board, the inverter, and a stand-alone computer. The analog signal interface PCB includes an output control for the inverter and two analog-to-digital (A/D) converters for converting load currents and voltages. The FPGA was programmed with XILINX® software (embedded in the Simulink® model) and used to drive the inverter.

D. THESIS ORGANIZATION

The purpose, research goals and the organization of the thesis were given in this chapter. The voltage source inverter major components, design, hardware, software and background information on VSI conversion principles are given in Chapter II. Construction, testing and interfacing the three-phase source inverter circuit board are explored in Chapter III. The results, conclusions and future research opportunities are presented in Chapter IV. The PCB Schematics are in Appendix A. The MATLAB code for simulation data are presented in Appendix B. Information on the SEMITEACH® voltage inverter is provided Appendix C.

E. CHAPTER SUMMARY

A brief introduction of the three-phase voltage source inverter objectives, research goals, and the approach taken to meet those goals were given in this chapter. The theory of operation, the hardware and software interfaces used with the source inverter are introduced Chapter II.

II. BACKGROUND INFORMATION

A. INTRODUCTION

The theory of operation of the three-phase source inverter is covered in this chapter. The theory of operation, the major parts of the three-phase voltage source inverter, their interaction with other components and its interface with the FPGA are discussed.

B. THEORY OF OPERATION

1. Overview

An inverter, a critical component of most large motor drive systems, converts a dc power source into a controlled sinusoidal input current for an ac motor at a desired operating frequency. The dc power can be produced by rectifying an ac source. The inverter uses a network of solid-state switches to alternate between the positive and negative input dc source to produce the ac voltage across the load [4]. A simple half bridge inverter is depicted in Figure 1.

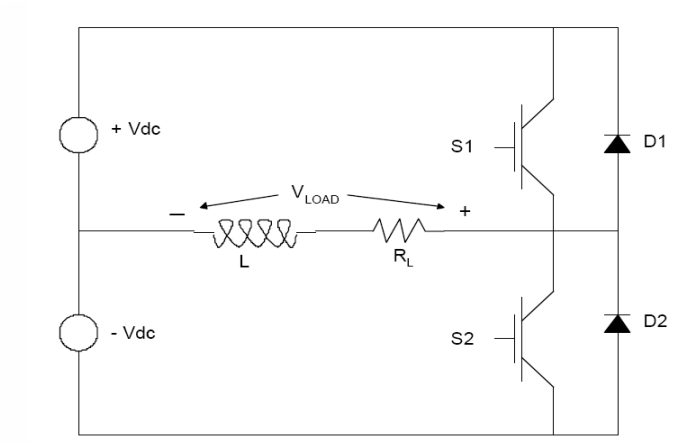


Figure 1. Simple half-bridge inverter.

The inverter’s sinusoidal amplitude and frequency output can be directly controlled by timing the opening and closing of switches S1 and S2.

The IGBT is an example of a type of solid-state switch commonly used for inverters. The quality of the output waveform is dependent on a number of variables that include the relative switching frequency speed and is generally specified in number of pulses (or switchings) per half-cycle of the output fundamental voltage or current [4]. For most loads, the ideal voltage and current waveforms are sinusoidal at the desired operating frequency. For nonlinear loads, it is common to force the voltage to be sinusoidal while letting the load characteristics define the output waveform.

Given a fixed amount of filtering and sufficient control bandwidth, the switching sequence, including the relative rate at which the switches operate, determines the inverter’s output accuracy when following a reference sinusoid. As a result, the output of an inverter at a lower relative switching frequency does not match the desired sinusoidal pattern as closely as an inverter switching at a higher frequency. Non-sinusoidal waveforms are rich in harmonic content not directly usable by a machine load. The total harmonic content that is not directly usable by a machine load is known as the total harmonic distortion (THD) of the current. The THD should be minimized to alleviate unwanted noise from torque pulsations and excess heating from eddy current losses.

The load current waveform $I_{L(t)}$ can be represented by a composite series of the fundamental component and the sum of the higher harmonic components and is given by [4]

$$I_L(t) = I_{L1}(t) + \sum_{h\neq 1}^{\infty} I_{Lh}(t) \,. \tag{2.1}$$

The first term (I_{L1}) is the desired fundamental frequency component, while the summation of the I_{Lh} terms represents harmonic content. Ideally, the harmonic terms are zero for a perfectly sinusoidal waveform at the fundamental frequency. The root-mean-squared (RMS) value of the current waveform is given by [4]

$$I_L = \sqrt{I_{L1^2} + \sum_{h\neq 1}^{\infty} I^2{}_{Lh}} \,. \tag{2.2}$$

The actual distortion present in the current waveform due to its harmonics can be derived from the above relations. The THD as a percentage of the total current waveform is given by [4]

$$\%THD = 100\sqrt{\sum_{h\neq 1}^{\infty}\left(\frac{I_{Lh}}{I_{L1}}\right)^2} \,. \tag{2.3}$$

The objective of the inverter system is to minimize the THD to match a sinusoidal reference signal as closely as possible.

Various methods can be employed to control the switches within the inverter to produce an ac output current. The objective of any switching control scheme is to sequence the switches to match the desired reference signal. Some switching schemes are very simple, while others are quite complex and require the use of microprocessors and FPGAs.

The simplest of switching methods for inverters is square-wave switching. With this method, the inverter cycles the voltage across the load by alternating the positive dc voltage and then the negative dc voltage at the desired output frequency. This method closes the top switch (S1 in Figure 1) when the reference signal is positive and closes the bottom switch (S2 in Figure 1) when the reference signal is negative. Although easy to implement, the square-wave switching method produces an output waveform that falls short of matching the sinusoidal reference signal. Consequently, the THD of the voltage is 47.8% and 30.5% for single-phase and three-phase, respectively [4]. The distortion in the current is based on the significant amount of harmonic current in the output.

A more complex but commonly used switching scheme is called pulse-width modulation (PWM). PWM techniques are capable of producing a good representation of the desired waveform with only the inclusion of higher, easily filterable, harmonics at the switching frequency. With PWM, the positive or negative dc input source voltage is applied to the load in pulses of varying length at a frequency much higher than the fundamental frequency. While the amplitude and frequency of the pulses is fixed, the width of the

individual pulses is weighted by multiplying a reference waveform by a higher frequency triangular-carrier to produce a digitized representation of the reference.

A more complex and widespread technique for inverter control is sine-PWM. In a sine-PWM inverter, a sinusoidal reference signal of the desired output frequency is compared to a triangular modulation signal at a much higher frequency.

The resultant applied voltage levels for a typical cycle in a sine-PWM inverter is depicted in Figure 2.

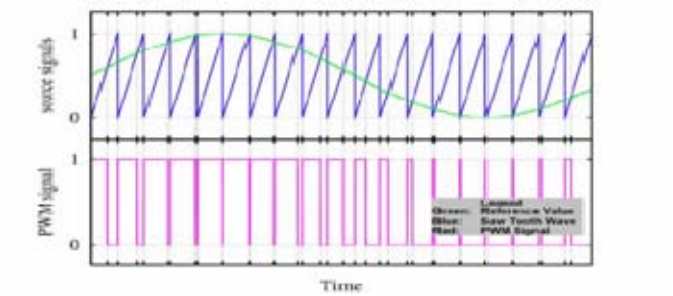


Figure 2. Typical sine-PWM applied load voltage (From: [5]).

The controller, typically an FPGA or microprocessor, uses a constant frequency to switch the inverter IGBT. This process, as stated earlier, is known as PWM, as shown in Figure 2. It uses a reference signal, shown in Figure 2, to compare to a constant frequency saw-tooth waveform. When the reference signal is of a higher value than the saw-tooth waveform, the FPGA controller sends out a “high” or “on” signal to the inverter top IGBT switch. When the reference signal is of lower value than the saw-tooth waveform, the FPGA controller sends out a “low” or “off” signal to the upper inverter IGBT switch and turns on the

bottom switch. In Figure 2, the resulting signal from the constant comparison of the reference signal to the saw tooth waveform is shown as red. As can be seen, the PWM signal is a square-wave signal of varying duty cycle that operates at the same frequency as that of the saw tooth waveform. This type of inverter can produce a very high fidelity current waveform and its use is widespread. The two control signals (pulse-width modulation reference and carrier signals) and the switching scheme are illustrated in Figure 2.

A brief description of the algorithm to control the applied voltage to the load is as follows.

If Vref > Vtri:

Close S1 (top switch), open S2 (bottom switch)

Set VLOAD to + Vdc.

If Vref < Vtri:

Open S1 (top switch), close S2 (bottom switch)

Set VLOAD to – Vdc.

For this thesis, a three-phase VSI was designed [6]. The VSI was developed to generate a three-phase ac power supply from a single-phase ac supply. An FPGA controller is used to control the voltage source inverter to generate a third voltage, which along with the single voltage from the supply, creates a balanced three-phase ac to drive the motor. The newly developed three-phase VSI was designed as a compact, cost optimized, and readily available

alternative to the current system at NPS using IPM IGBTs as identified in Chapter I. A simple block diagram of a basic inverter using the new ST IPM IGBT device is shown in Figure 3.

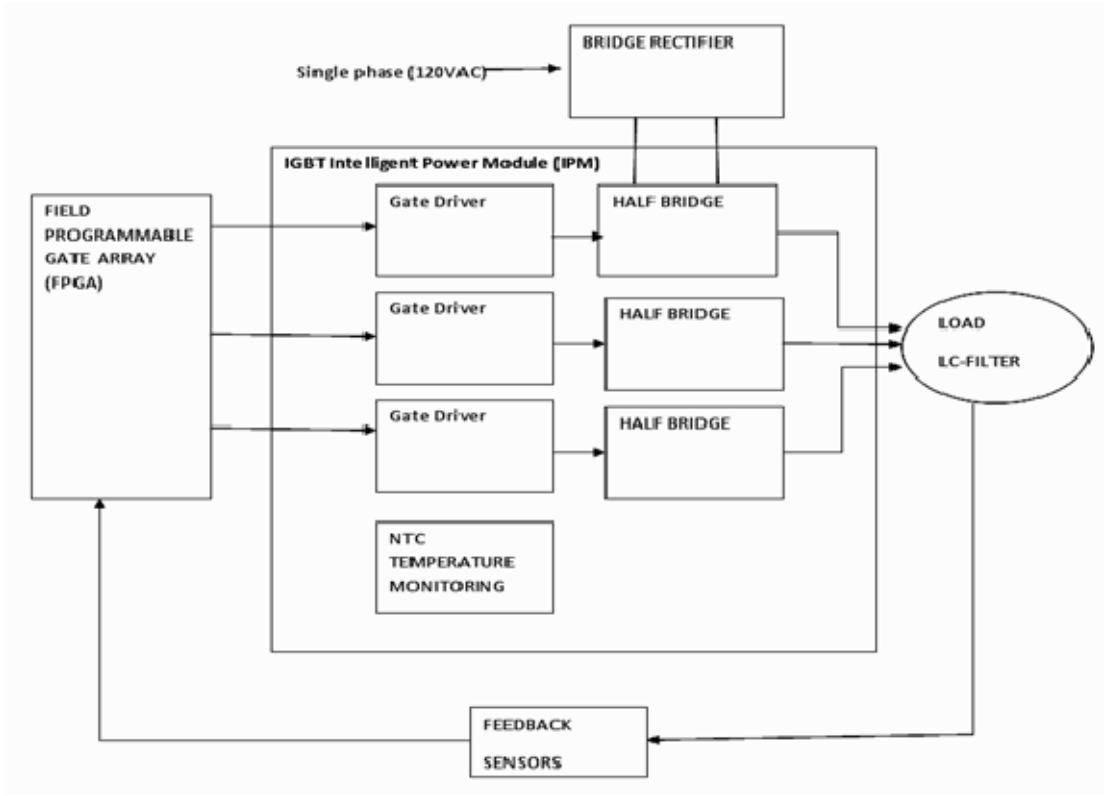


Figure 3. VSI IPM module diagram.

2. Voltage Source Inverter

The VSI printed circuit board discussed in this thesis operates by converting single-phase ac power from the wall outlet to dc and then back to three-phase ac using an IGBT inverter. In the three-phase voltage source inverter, the rectified dc power from a wall outlet is fed into the three half bridges in series with an LC filter with a delta configured capacitor bank to run a three variable resistors

load in delta configuration. The IGBTs are controlled by the FPGA through the gate drivers. The inverter consists of six IGBTs, which creates an ac voltage by drawing on the power of the dc bus. The amplitude and frequency of the sinusoidal waveform can be controlled directly by properly timing the opening and closing of the IGBT switches. The quality of the output waveform is dependent on a number of variables including the relative switching frequency, the filtering, and the bandwidth of the FPGA controller. Voltages created by the IGBT power switching are not sinusoidal but are pulse width modulated waveforms with high harmonic distortion. The PWM voltages are then passed through a LC filter network to produce a sine wave with less distortion. The FPGA monitors and adjusts the generated voltage to produce a constant, balanced three-phase voltage. The IPM is also embedded with a protective smart shut down function in case of over-voltage, under-voltage, or fault. With the ability to adjust to changing conditions, the three-phase voltage source inverter can operate safely and effectively on three-phase systems. A pictorial view of the new VSI is shown in Figure 4.

Figure 4. VSI printed circuit board.

C. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

A field programmable gate array is a semiconductor device containing programmable logic components and programmable interconnects. The programmable logic components, such as AND, NOR, OR and XOR gates and other complex logic, can be programmed to duplicate the functionality of basic logic gates or more complex combinational functions [7]. In this case, the FPGA function is used to readily and effectively control the switching of the IGBTs and also provide the required signals to drive the voltage and current sensors. A major advantage of this technology is that FPGAs can execute code in parallel. FPGAs can be thought of as a Table-of-Equations executed simultaneously (when feasible) during a given clock cycle and they have traditionally been used in high-speed custom digital applications where designs tend to be more constrained by performance. Their widespread use and reduction in price makes them the controller of choice in embedded applications, such as the VSI. The number of parallel calculations is limited by the size of the FPGA.

Current technology produces speeds up to 600 MHz in certain designs; however, the SDC operates at 25 MHz using only a fraction of this speed [7],[8].

XILINX®, a leading manufacturer of FPGAs, primarily builds array-based circuits. These circuits incorporate chips comprised of two-dimensional arrays of logic blocks that can be interconnected via horizontal and vertical routing channels [7]. The XILINX® Virtex-4™ development board is shown in Figure 5.

Figure 5. XILINX® Virtex-4™ development board (From: [7]).

The Virtex-4™ was designed as a user-friendly platform for prototyping, simulating, testing and verifying designs. A high-level block diagram of the Virtex-4™ is shown in Figure 6.

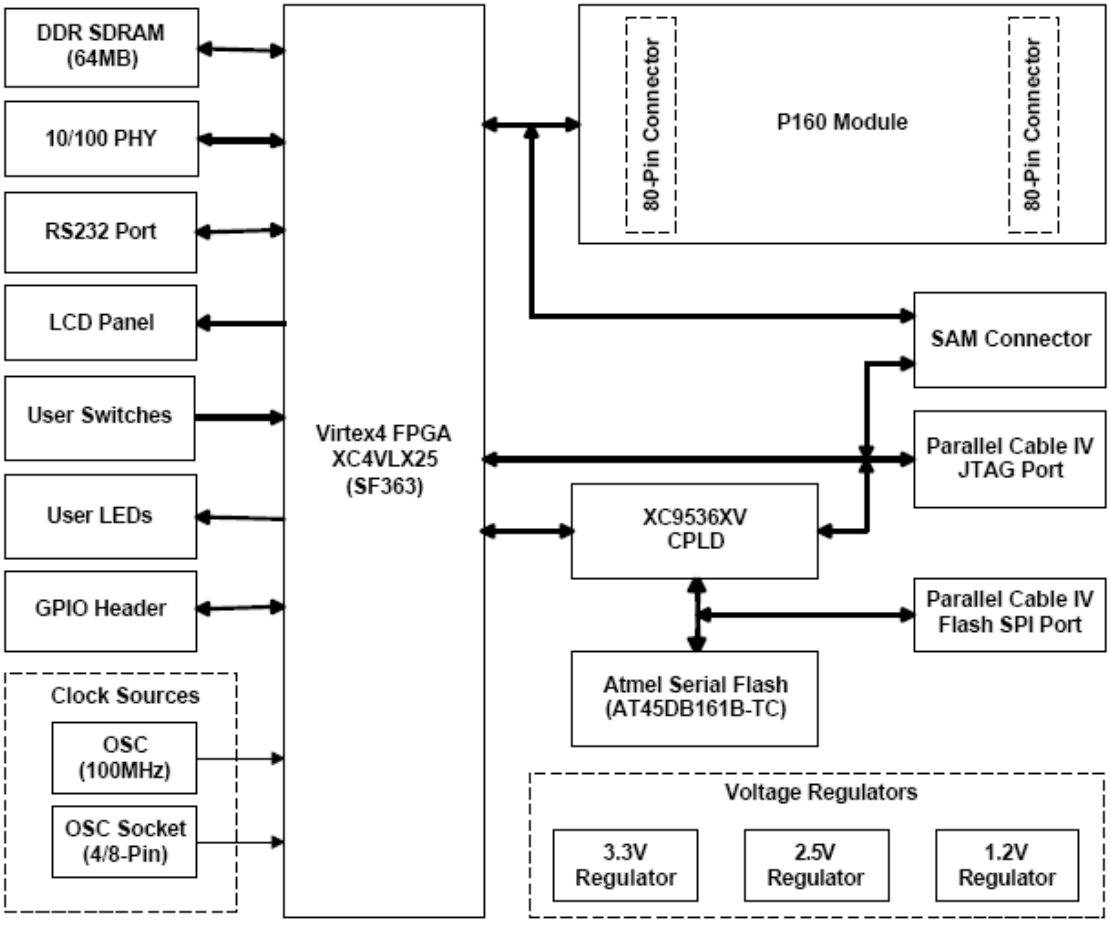


Figure 6. High-Level block diagram of the Virtex-4™ (From: [7]).

D. HARDWARE INTERFACE USING CHIPSCOPE™ PRO

Chipscope interface software is a computer-based interface that communicates with the FPGA through the JTAG ports. The Xilinx Chipscope block can be accessed at run-

time using the Chipscope pro analyzer software. The analyzer configures the FPGA, sets up trigger conditions and views data run-time. Chipscope is a PC accessible software able to program, interact with, export data from the FPGA and read back into the MATLAB workspace, making it particularly useful throughout the design, simulation and testing of the voltage source inverter. The user can remotely control the inverter through the computer using ChipScope™ Pro software. ChipScope™ Pro inserts a logic analyzer, bus analyzer, and virtual I/O low-profile software core directly into the design. This allows the user to view any internal signal or node, including embedded hard or soft processors. Signals are captured at or near operating system speed, and the process is limited only by the speed of the acquisition of analog signals in digital form [7],[8]. The data is then viewed through the programming interface and analyzed with the ChipScope™ Pro Logic Analyzer [7].

The virtual input-output (VIO) console in the software allows the user to control the hardware. For example, one bit can be toggled to turn the converter on and off.

In this manner, the user can remotely control the FPGA, and thus, the voltage conversion process, using ChipScope™ Pro. Detailed analyses of input and output signals can be accomplished digitally; hence, an oscilloscope is no longer necessary for laboratory measurements. The user can evaluate a signal bit-by-bit if necessary. Furthermore, calibration of the sampled signal

can be accomplished by adjusting gain blocks in the Simulink® model. The next chapter explains this feature in more detail.

E. CHAPTER SUMMARY

An overview of the VSI board was presented with a brief background of the voltage conversion process, the new IGBT IPM, FPGA and software utilization process. The development, construction, and testing of the printed circuit board and experimental thermal analysis conducted using the Celsius temperature sensor are covered in the next chapter.

THIS PAGE INTENTIONALLY LEFT BLANK

III. PRINTED CIRCUIT BOARD DESIGN AND TESTING

A. SCHEMATIC DESIGN

PCB123 software was used to create and prepare the board schematics and layout [6]. Individual components were manually placed on the board, and prior to energizing, a system check was done to verify continuity.

The circuit diagram in Figure 7 depicts the major components of the system.

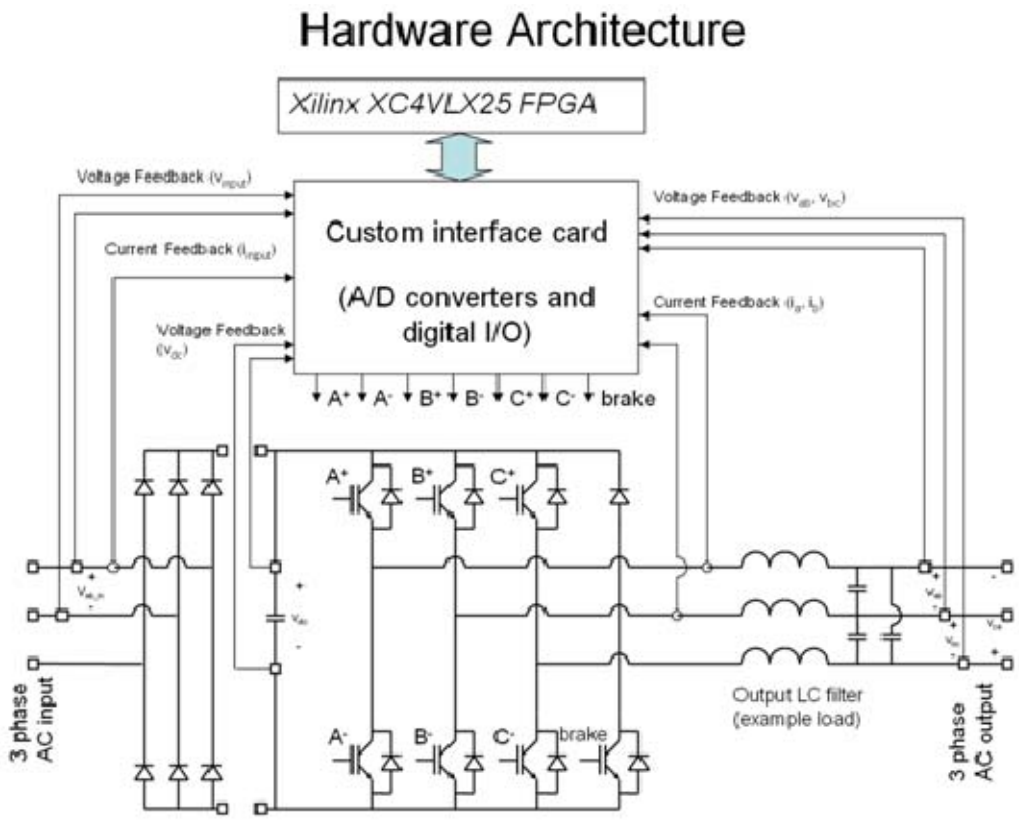


Figure 7. Schematic diagram of the VSI laboratory hardware architecture.

The VSI design is given in [6]. It consists of the new intelligent IPM module as the main part of the system. The main components are the following: six pack IPM module, voltage rectifier, optocouplers, FPGA interface jacks, and voltage and current sensors.

The IPM IGBT is a three-phase inverter with the output connected in series with an inductor and then connected to a delta configuration of capacitors to produce an LC filter load. The value of the LC filter and the load resistor is adjusted to be equal to the computer-simulated values. The LC filter limits the current and the voltage in the time domain to produce a low pass filter.

B. THERMAL ANALYSIS

To utilize the newly developed VSI IGBT IPM module fully, sufficient attention must be paid to proper heat removal of the IGBT. The IGBT IPM will have conduction and switching power losses. The heat generated as a result of these losses must be conducted away from the power chip and into the environment using a heatsink. For efficient thermal management, the user must rely on important parameters supplied by the manufacturer, such as junction-to-case and junction-to-ambient thermal resistances and maximum operating junction temperature. The device temperature depends on the power dissipation level, the means for removing the heat generated by this power dissipation and the temperature of the body (heat sink) to which this heat is removed.

A simplified equivalent circuit for a typical semiconductor device in equilibrium is shown in Figure 8.

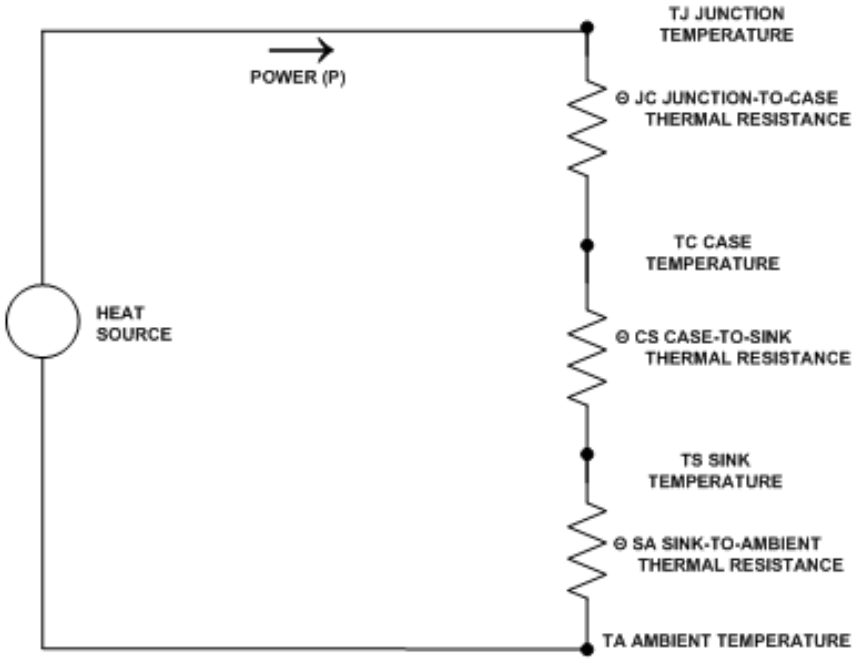


Figure 8. Simplified thermal circuit.

The power dissipation, which is analogous to current flow in electrical terms, represents the heat source. Temperature is equivalent to voltage potential and thermal resistance to ohmic resistance. If θ_{JA} is the junction to ambient thermal resistance, θ_{JC} is the junction-to-case thermal resistance, θ_{CS} is the case-to-sink thermal resistance and θ_{SA} is the sink-to-ambient thermal resistance, then the total required thermal resistance is given by

$$\theta_{JA(total)} = \theta_{JC} + \theta_{CS} + \theta_{SA} = \frac{T_J - T_A}{P_D} \; . \qquad (3.1)$$

The rise in the temperature of a package above some reference level per unit of power dissipation is expressed in degrees Celsius per watt. Several factors affect thermal resistance including die size, the size of the heat source on the die (series-pass transistor in an IC regulator), die-attach material and thickness, lead frame material, and construction and thickness.

To measure thermal resistance, the difference between the junction temperature and the chosen reference temperature, case, sink or ambient, must be determined. An ambient or sink temperature measurement is straightforward. For a case-temperature measurement, the device should have a sufficiently large heat sink. Measurement of the junction temperature, unfortunately, is not as simple and involves some approximation as practical as possible [9].

The thermal behavior analysis of a three-phase VSI developed at NPS is covered in this section. The thermal analysis is an ongoing research effort; its benefits include increasing reliability by estimating the thermal impedance of the IGBT module. Estimation of thermal impedance quantifies the characteristics of the heat sink needed to dissipate the heat under worst-case conditions. The IPM IGBT is embedded with a temperature-monitoring surface. The setup of the LM 35 temperature sensor consists of a 5V power supply, a ground connection and a multimeter readout on the output. An LM35 chip is mounted on the heat sink and a typical application connection shown in Figure 9.

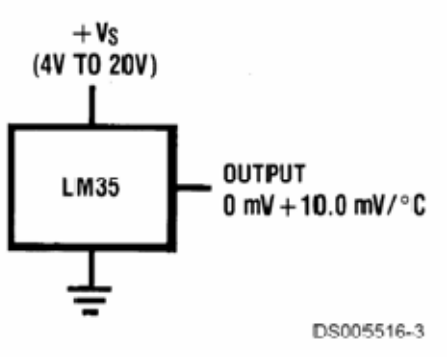


Figure 9. LM 35 basic Celsius temperature sensor (From: [10]).

Based on the setup shown in Figure 9, the following measurements in Table 1 were obtained and plotted by MATLAB. The experimental data measurement shown in Table 1 provides the relationship between measured temperature and voltage values, which are 10mV/C.

Table 1. Thermal behavior analysis data.

Thermal Behavior analysis Data(LM35 on IGBT IPM Heat sink)				
$R_{LOAD}(\Omega)$	voltages(mV)	Time (Seconds)	Temperature (Celsius)=mV/10	Remarks
240	230mV	0	23	**LM 35 Precision Centigrade Temperature Sensor Gain: OUTPUT up to 10mV per Celsius 10mV/C**
240	304mV	60	30.4	
240	370mV	120	37	
240	399mV	180	39.9	
240	434mV	240	43.4	
240	460mV	300	46	
240	490mV	360	49	
240	508mV	420	50.8	
240	524mV	480	52.4	
240	529mV	540	52.9	

A plot of temperature versus time showing an exponentially rising temperature that reaches equilibrium after 500 seconds is shown in Figure 10.

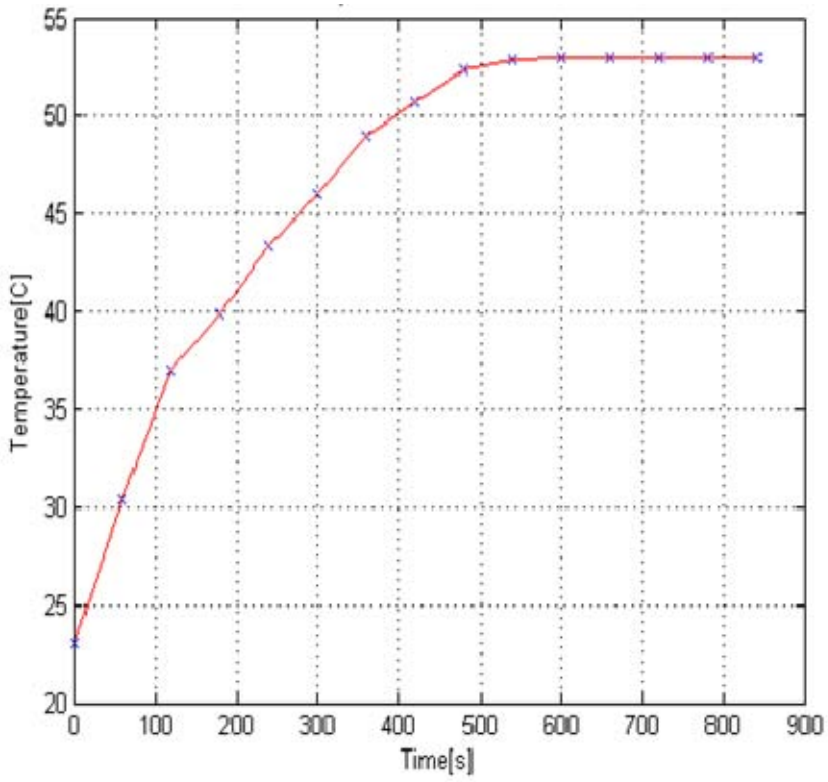


Figure 10. Temperature vs. time for the IGBT IPM heat sink.

Due to various implementations of new design features on newer ships and electric load distributors, thermal issues are increasingly becoming a problem. The shrinking component sizes result in greater surface in many devices as material advances and switching speed of smaller electronics components reach new heights. Thus, these new devices require a significant innovation in cooling capacity.

The new VSI Intelligent IGBT semiconductor device was tested under various lab conditions. The experiment utilized the LM35 precision centigrade temperature sensor. Its low cost, low self-heating, low output impedance, linear output and precise inherent calibration make interfacing to the LM35 readout or control circuit especially easy [10].

Other experimental assumptions made due to their negligible effect are as follows:

- Each half-bridge inverter, including its free wheeling diode temperature drop from IGBT case to the heat sink, is neglected
- Thermal coupling between the IGBT and free wheeling diode is also neglected
- The thermal boundary, which represents the IGBT case to its package, is neglected due to the amount of surface area for heat to dissipate and thermal paste applied

The thermal and switching loss data used in this thesis are shown in Table 2.

Table 2. Thermal data from the manufacturer.

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case single IGBT	2.4	C/W
R_{thJC}	Thermal resistance junction-case single diode	5.0	C/W
R_{thJC}	Thermal resistance case-sink	4.6	C/W
E_{on}	Turn-on switching losses	290	μJ
E_{off}	Turn-off switching losses	250	μJ

The thermal equivalent circuit for the VSI is shown in Figure 11. In the thermal modeling diagram, T_S is the heat

sink temperature measured with the probe and P_{Loss} symbolizes the current source representing the injected power. The objective is to estimate the semiconductor junction temperature based on the estimated thermal impedance for the mechanical system. This analysis is simplified by making the diode junction and the IGBT junction the same temperature, which is represented by a short circuit in Figure 11 from T_{IGBT} to T_{diode}. The thermal model in Figure 11 relates to Figure 9 if assuming θ_{CS} is zero and two semiconductors are in parallel (θ_{JC} for the diode and transistor).

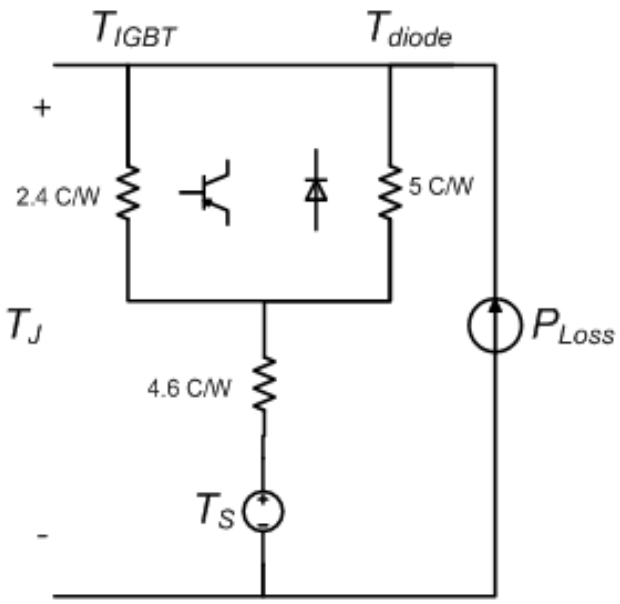


Figure 11. Thermal model of the IGBT IPM heat sink.

The IGBT inverter module was operated under the following conditions: V_{dc}=155V, $F_{switching}$=10 KHz, and I_{RMS}= 0.8990A.

The temperature measured on the heat sink was 50C. The estimated losses for this operating condition are shown in Table 3.

1. RMS in Frequency Domain

The RMS was computed using Parseval's theorem for the sampled signal in Figure 12.

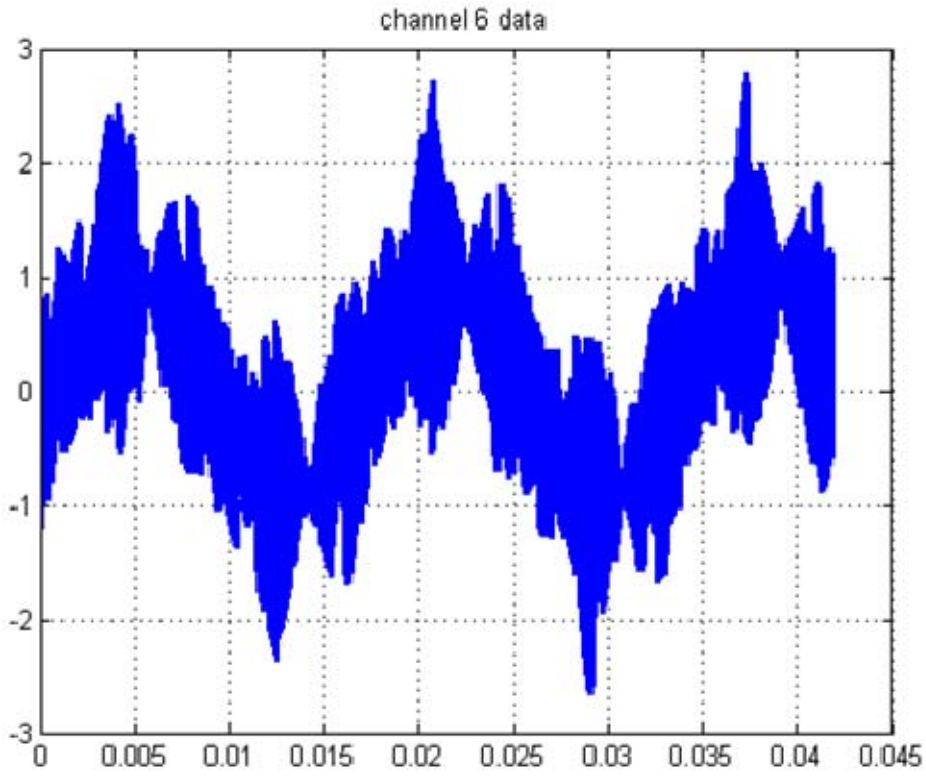


Figure 12. Sample current waveform from Chipscope.

The I_{RMS} was calculated given

$$I_{RMS} = \sqrt{((1/length(timedata)\sum(ch6\,final.^2))} \; . \qquad (3.2)$$

The I_{RMS} = 0.899A was calculated using Equation (3.2) and the MATLAB data provided in Appendix C.

The power losses P_{toatal} are the sum of the conduction losses and the on/off or switching losses as given by

$$P_{total} = P_{cond} + P_{switch} \tag{3.3}$$

where P_{cond} represents conduction losses while the IGBT is on and conducting current and P_{switch} is the power dissipated during the turn-on and turn-off switching transition.

The switching losses P_{switch} are the product of the turn on/off energy dissipated in the IGBT and the switching frequency, which is multiplied by six to account for six IGBTs. For an IGBT, the switching losses are

$$P_{switch} = (E_{on} + E_{off})\, f_{sw} \tag{3.4}$$

where E_{on} is the turn-on switching energy, E_{off} is the turn-off switching energy and f_{sw} is the switching frequency (see Table 2).

The conduction losses P_{cond} are estimated by multiplying the average forward voltage drop of the semiconductors times the RMS current. This quantity is multiplied by three since there are three half bridge legs in the VSI. For each IGBT/diode pair, the losses are

$$P_{cond} = \left(\frac{V_{ce} + V_d}{2}\right) I_{RMS}\, \frac{1}{2} \tag{3.5}$$

where V_{ce}=2.2V and V_d=3.8V. The calculated power dissipation values are shown in Table 3.

Table 3. The power dissipation table for each IGBT.

$I_{RMS}(A)$	$P_{Total}(C/W)$	$P_{switch}(W)$	$P_{cond}(W)$
0.8990	6.75	5.40	1.35

The average device voltage is used as an approximation of the semiconductor voltage drop.

The estimated temperature from the junction to the heat sink is 42.5C. A measurement of 50C at the heat sink predicts that the junction temperature is 92.5C in this operating mode. The thermal impedance is computed from Figure 11. The thermal impedance is multiplied by the power dissipated by one diode/IGBT pair to find the junction temperature above the heatsink temperature. Evaluating Equation (3.1) for the temperature rise obtains

$$\left(\frac{2.4*5.0}{7.4}+4.6\right)*6.75 = 42.5^{o}\mathrm{C} = \mathrm{T}_J\text{-}\mathrm{T}_S\ . \qquad (3.6)$$

The allowable IGBT junction temperature is 125C; enhance, the thermal analysis predicts that the device is not overheating.

C. VOLTAGE SENSOR ANALYSIS

The voltage sensor's circuit diagram is shown in Figure 13. The power dissipation in each resistor of the dc voltage sensor is computed in Table 4. The calculated power for each resistor in the ac voltage sensors is summarized in Table 5. The resistors and capacitor shown in Figure 13 form a lowpass filter. The filter gain and phase shift are plotted in Figures 14 and 15, respectively.

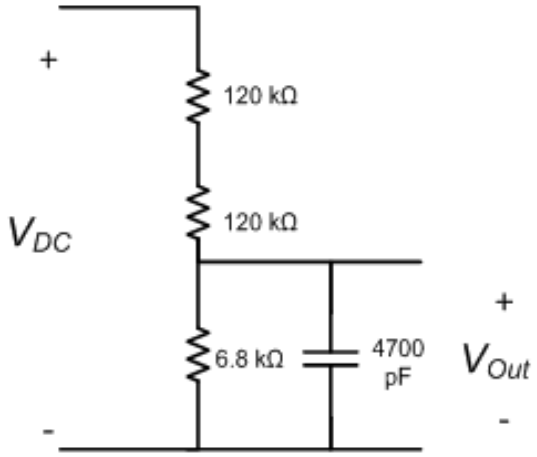


Figure 13. DC bus sensor.

The dc bus sensor with three resistors: $120K\Omega$, $120K\Omega$, and $6.8K\Omega$ is shown in Figure 13. The dc bus voltage is designed to be as high as $350V_{dc}$. The dc current is given by

$$I_{dc} = (V_{\max}^2 / R_{total}) . \quad (3.7)$$

For dc, I_{dc}=350/(120+120+6.8)kΩ=1.42mA and the dissipated power per resistor is given by

$$P_{dc} = (I_{dc}^2 R) . \quad (3.8)$$

Table 4. Calculated dc bus sensor tables.

Resistor	R1	R2	R3
Resistor Values (ohms)	120	120	6.8
$P_{dc} = (I_{dc}^2 R)$	242mW	242mW	14mW

The ac output voltage is designed to be as high as 220 Vac. AC sensor resistances are 56kΩ, 56kΩ, and 3kΩ and the R_{total} is the sum of the three sensor resistors. The power dissipated on each ac sensor resistor shown in Table 5 is given by

$$P = (I_{RMS}^2 R_{total}) . \quad (3.9)$$

A 2mA I_{RMS} current is given by

$$I_{RMS} = (V_{RMS} / R_{total}) . \quad (3.10)$$

Table 5. Calculated ac sensor tables.

Resistor	R1	R2	R3
Resistor Values (ohms)	56	56	3
Power	224mW	224mW	17mW

1. Low Pass Filter MATLAB Code

The filter corner frequency is shown to be about 10 KHz in Figure 14. The filter gain and phase shift plotted for the ac voltage sensor using MATLAB are depicted in Figures 14 and 15. The power dissipated in each resistor is shown in Table 5.

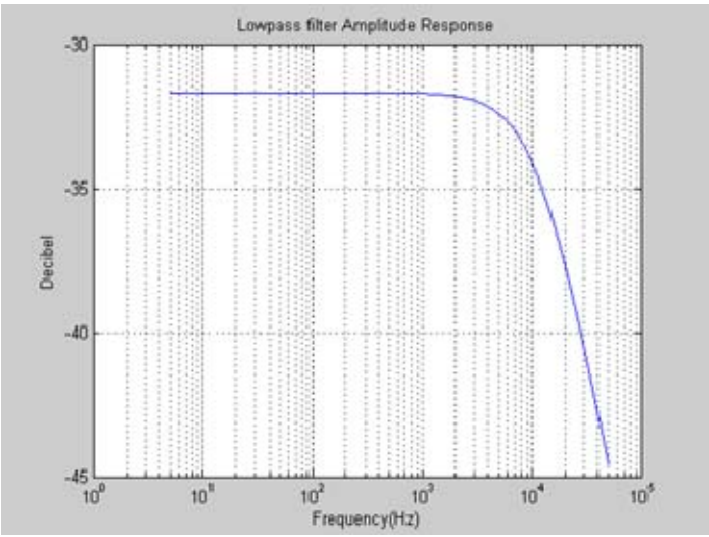


Figure 14. Lowpass filter amplitude response.

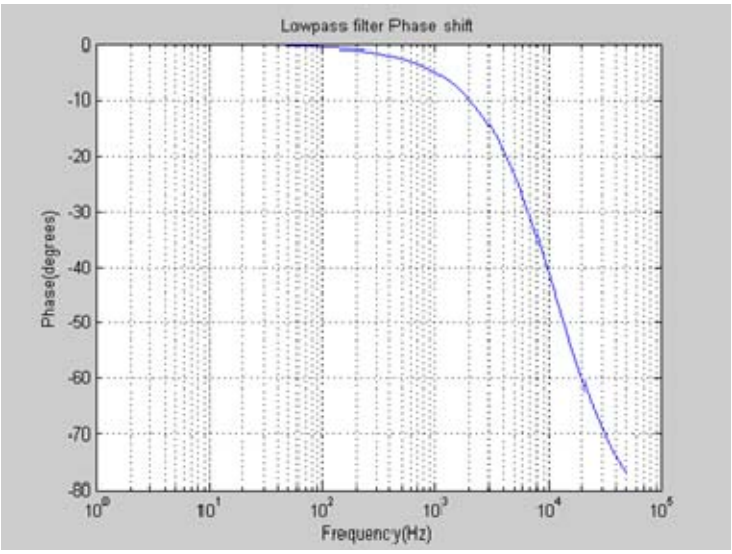


Figure 15. Lowpass filter phase shift.

The lowpass filter passes low-frequency signals but attenuates or reduces the amplitude of the signals above the cutoff frequency. A lowpass filter consists of a resistor in series with a load, and a capacitor in parallel with the load. The capacitor exhibits reactance, and blocks low-frequency signals, causing them to go through the load

instead. At higher frequencies, the reactance drops, and the capacitor effectively functions as a short circuit. The combination of resistance and capacitance provides the time constant of the filter $\tau = RC$. The cutoff frequency (in hertz), is given by

$$f_c = \frac{1}{2\pi RC}. \tag{3.11}$$

The transfer function for the lowpass filter is

$$H(j\omega) = \frac{R_3 \| \frac{1}{j\omega C}}{R_1 + R_2 + R_3 \| \frac{1}{j\omega C}} \tag{3.12}$$

where R_1, R_2 and R_3 represents the impedance of the resistors and $\frac{1}{j\omega C}$ represents the impedance of the parallel capacitor.

At $4700\,pF$, the cutoff frequency is approximately 10 kHz.

2. Current Sensor

The current sensor gain is 1/333 and the burden resistor is 330Ω ohms. Thus, the current sensor output signal is 330V/333A. The connection option used in this thesis is shown in Table 6.

Table 6. 25_NP transducer datasheet connection option.

Number of primary Turns	Primary Current		Nominal Output current	Turns Ratio	Primary Resistance	Primary insertion Inductance	Recommended PCB connections
	Nominal	maximum					
	I_{PN} [A]	I_F [A]	I_{SN} [mA]	K_n	R_p [mΩ]	L_p [μH]	
3	8	18	24	3 : 1000	1.62	0.110	3 2 1 IN  OUT 4 5 6

The internal connections of the LAH 25_NP current transducer are shown in Figure 16. A current of 10A yields a 10V signal with a 3:1000 turns ratio (K_n) and a 333Ω burden resistor (R_m in Figure 16). Connection of the current sensor so that a turns ratio of 3/1000 is achieved is explained in Appendix B.

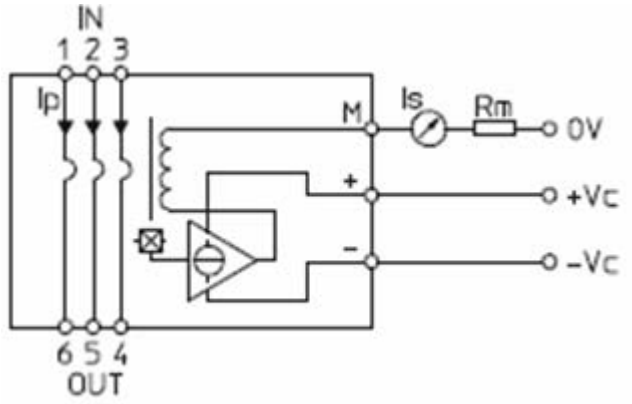


Figure 16. Internal schematic of the current transducer (From: [11]).

3. Optocouplers

Optocouplers are used for electrical isolation. It generally consists of a light emitting diode (LED) and a photodiode in one opaque package. The functional block

diagram and schematic of the FOD2220 optocoupler is shown in Figure 17. The FOD2220 is an optically coupled logic gate that combines an aluminum gallium arsenide (ALGaAS) LED and an integrated high gain photo detector for electrical isolation [12].

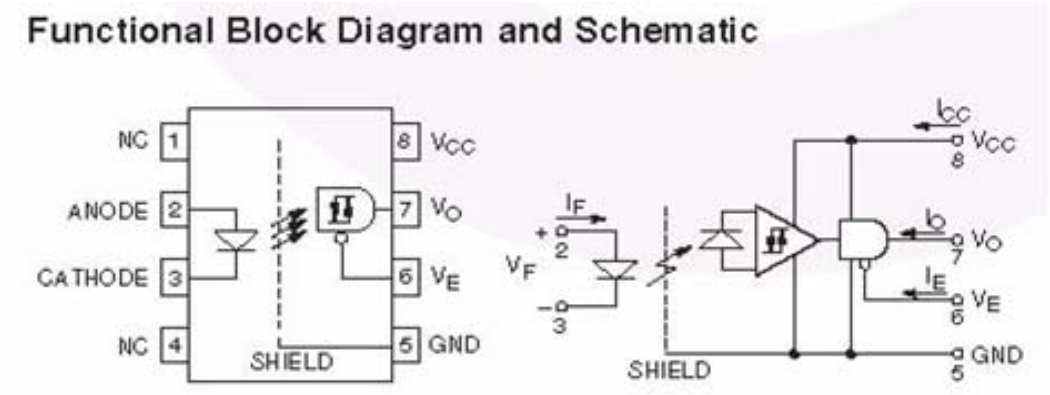


Figure 17. Schematic diagram of optocoupler (From: [12]).

The gate drive signals coming from the FGPA are isolated from the VSI and are sent to the VSI through optocouplers. This is necessary because the ground references for the gate drive control signals in the VSI are the negative DC bus, which can be as much as 350 volts away from earth ground or logic ground from the FPGA.

D. CHAPTER SUMMARY

An overview of the IGBT thermal behavior analysis, printed circuit board construction and testing, and experimental results based on the thermal behavior analysis of the IGBT IPM were presented in this chapter. The summary of this thesis and topics for future research are presented in the next chapter.

THIS PAGE INTENTIONALLY LEFT BLANK

IV. CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY

This thesis began with an overview of the voltage source inverter. The purpose and function of each major component and interfaces was explained to develop a working knowledge of the inverter. The design and testing of a VSI and its interface circuit boards was discussed, and system performance testing was done to ensure EMI from the switching inverter did not inhibit signal sampling. Finally, a thermal experiment was performed on the IGBT heat sink to ensure reliable performance such that the heat sink was able to maintain the device temperature below the maximum allowable temperature specified by the manufacturer.

B. CONCLUSIONS

The development of the three-phase voltage source inverter is an excellent resource for establishing flexible research capability at NPS. Students gain a fundamental understanding of schematics, circuit design, the advantages of using an FPGA for the control of power systems and digital signal analysis using ChipScope™ Pro. Students are enabled to make accurate predictions of component behavior using software simulation, testing and verifying results. New programs and ideas can be implemented without changing hardware and increasing costs. Students in other curricula can also experiment with other power electronics design for control of electrical systems.

C. RECOMMENDATIONS FOR FURTHER RESEARCH

There are many ongoing research opportunities in the area of Intelligent Power IGBT Module for power systems. Ideas for further research include thermal management solutions for three-phase VSI switching method with high quality power and least heat dissipation, the development of VSI laboratories for other electrical engineering curriculum tracks using FPGA technology, and cost optimized research for intelligent power electronics and electrical systems to improve efficiency, reliability and reduced cost.

The reprogrammable nature of the FPGA hardware enables a large number of programs and systems to be explored without the cost of purchasing and installing new hardware. For this reason, electrical engineering students at NPS can gain significantly from the use of FPGA technology as a valuable tool for flexible research capability at NPS.

APPENDIX A. PCB SCHEMATICS

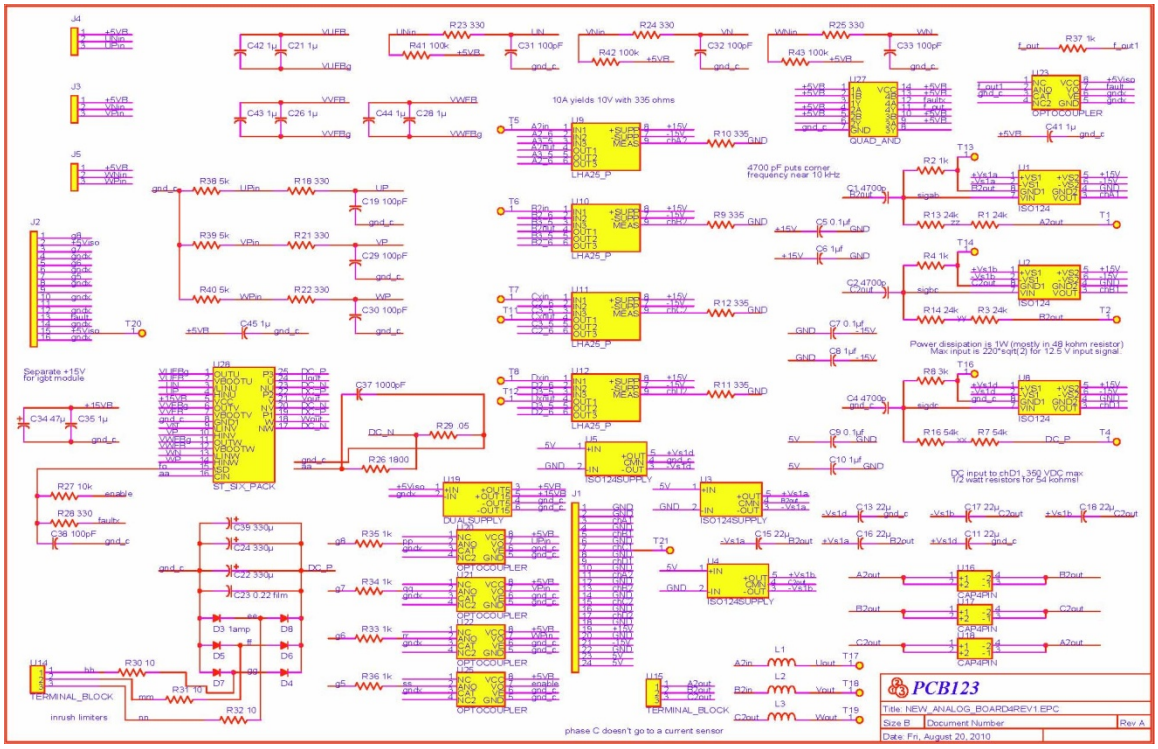


Figure 18. VSI schematic (From: [6]).

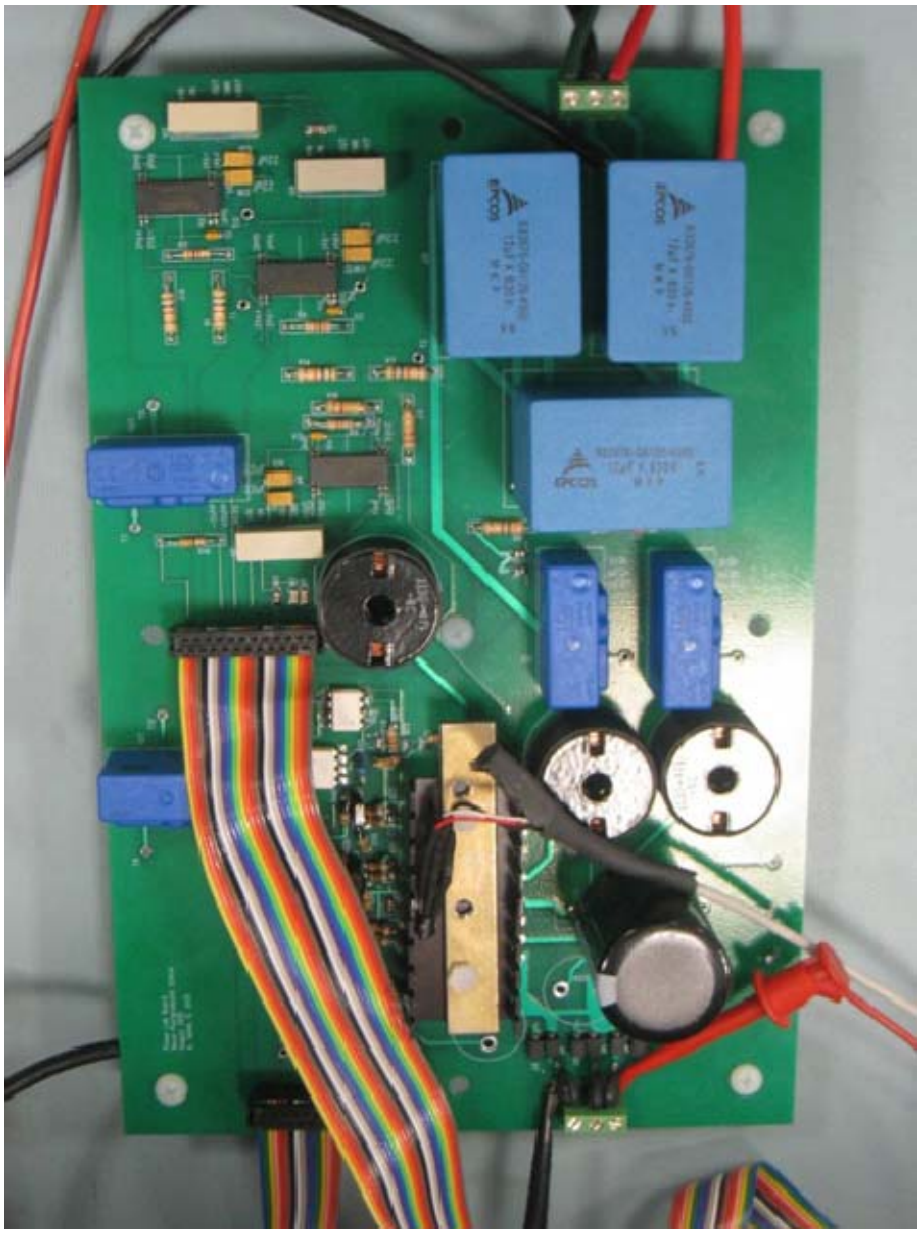
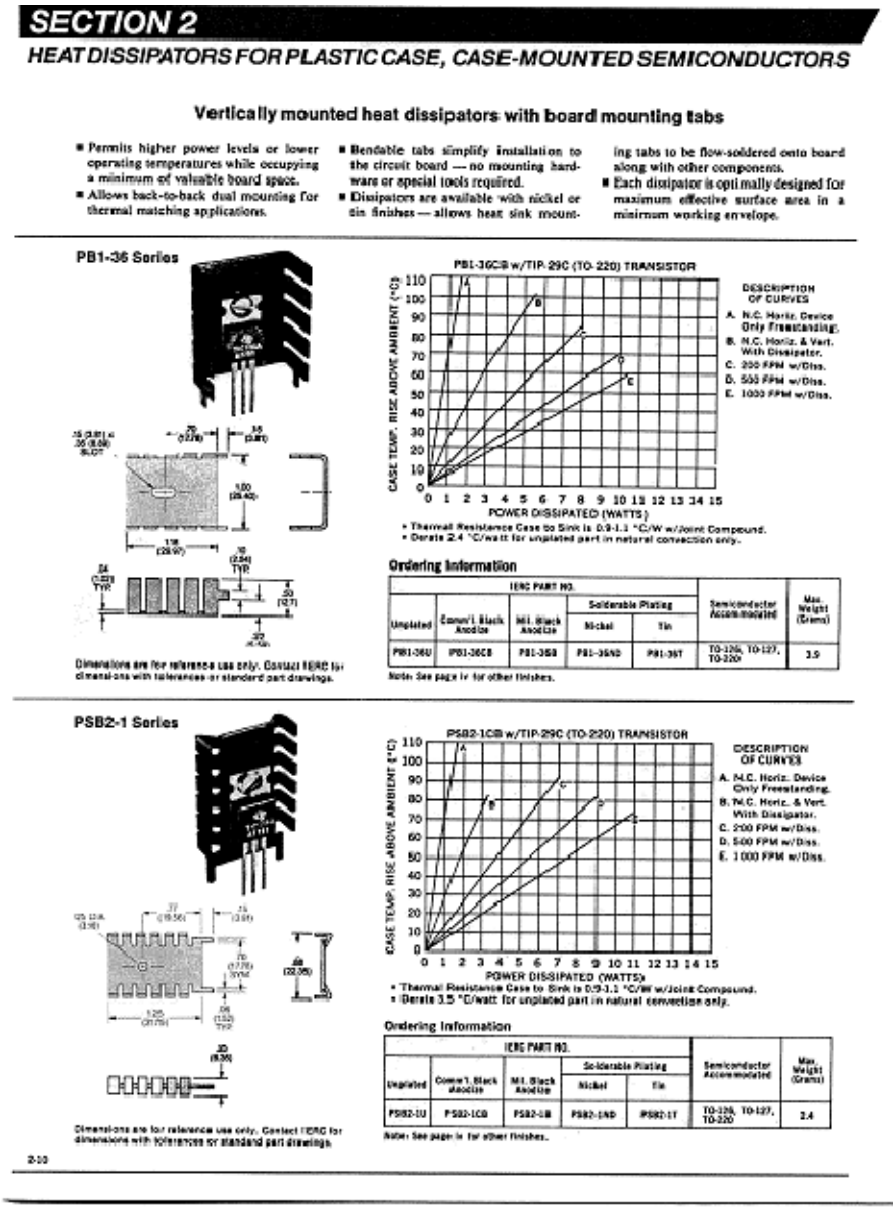


Figure 19. VSI printed circuit board.



SECTION 2

HEAT DISSIPATORS FOR PLASTIC CASE, CASE-MOUNTED SEMICONDUCTORS

Vertically mounted heat dissipators with board mounting tabs

- Permits higher power levels or lower operating temperatures while occupying a minimum of valuable board space.
- Allows back-to-back dual mounting for thermal matching applications.
- Bendable tabs simplify installation to the circuit board — no mounting hardware or special tools required.
- Dissipators are available with nickel or tin finishes — allows heat sink mounting tabs to be flow-soldered onto board along with other components.
- Each dissipator is optimally designed for maximum effective surface area in a minimum working envelope.

PB1-36 Series

PB1-36CB w/TIP-29C (TO-220) TRANSISTOR

CASE TEMP. RISE ABOVE AMBIENT (°C)

POWER DISSIPATED (WATTS)

DESCRIPTION OF CURVES

A. N.C. Horiz. Device Only Freestanding.
B. N.C. Horiz. & Vert. With Dissipator.
C. 200 FPM w/Diss.
D. 555 FPM w/Diss.
E. 1000 FPM w/Diss.

- Thermal Resistance Case to Sink is 0.9-1.1 °C/W w/Joint Compound.
- Derate 2.4 °C/watt for unplated part in natural convection only.

Ordering Information

IERC PART NO.					Semiconductor Accommodated	Max. Weight (Grams)
Unplated	Comm'l. Black Anodize	Mil. Black Anodize	Solderable Plating: Nickel	Solderable Plating: Tin		
PB1-36U	PB1-36CB	PB1-36B	PB1-36ND	PB1-36T	TO-126, TO-127, TO-220	3.9

Note: See page iv for other finishes.

Dimensions are for reference use only. Contact IERC for dimensions with tolerances or standard part drawings.

PSB2-1 Series

PSB2-1CB w/TIP-29C (TO-220) TRANSISTOR

CASE TEMP. RISE ABOVE AMBIENT (°C)

POWER DISSIPATED (WATTS)

DESCRIPTION OF CURVES

A. N.C. Horiz. Device Only Freestanding.
B. N.C. Horiz. & Vert. With Dissipator.
C. 200 FPM w/Diss.
D. 500 FPM w/Diss.
E. 1000 FPM w/Diss.

- Thermal Resistance Case to Sink is 0.9-1.1 °C/W w/Joint Compound.
- Derate 3.5 °C/watt for unplated part in natural convection only.

Ordering Information

IERC PART NO.					Semiconductor Accommodated	Max. Weight (Grams)
Unplated	Comm'l. Black Anodize	Mil. Black Anodize	Solderable Plating: Nickel	Solderable Plating: Tin		
PSB2-1U	PSB2-1CB	PSB2-1B	PSB2-1ND	PSB2-1T	TO-126, TO-127, TO-220	2.4

Note: See page iv for other finishes.

Dimensions are for reference use only. Contact IERC for dimensions with tolerances for standard part drawings.

2-10

Figure 20. Heat sink datasheet.

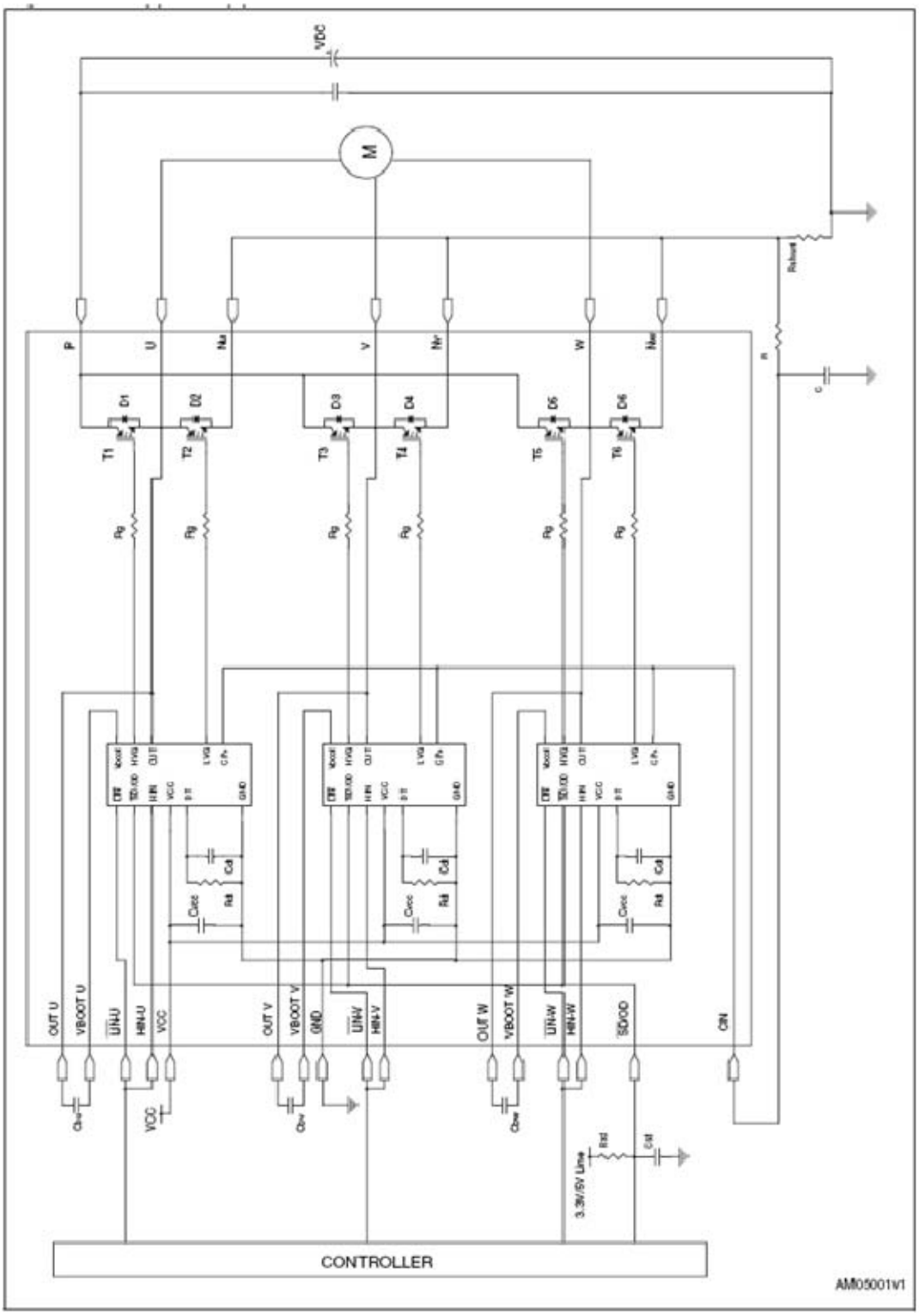


Figure 21. Typical application of STGIPS20K60.

5.1 Recommendations

- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The $\overline{SD}$/OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see *Section 4: Smart shutdown function* for detailed info).

Table 13. Recommended operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P-Nu, Nv, Nw		300	400	V
V_{CC}	Control supply voltage	Applied between V_{CC}-GND	13.5	15	18	V
V_{BS}	High side bias voltage	Applied between V_{BOOTi}-OUT_i for i=U, V, W			18	V
t_{dead}	Blanking time to prevent Arm-short	For each input signal	1			µs
f_{PWM}	PWM input signal	-40°C < T_C < 100°C -40°C < T_J < 125°C			20	kHz

Figure 22. STGIPS20K60 recommendations (From: [3]).

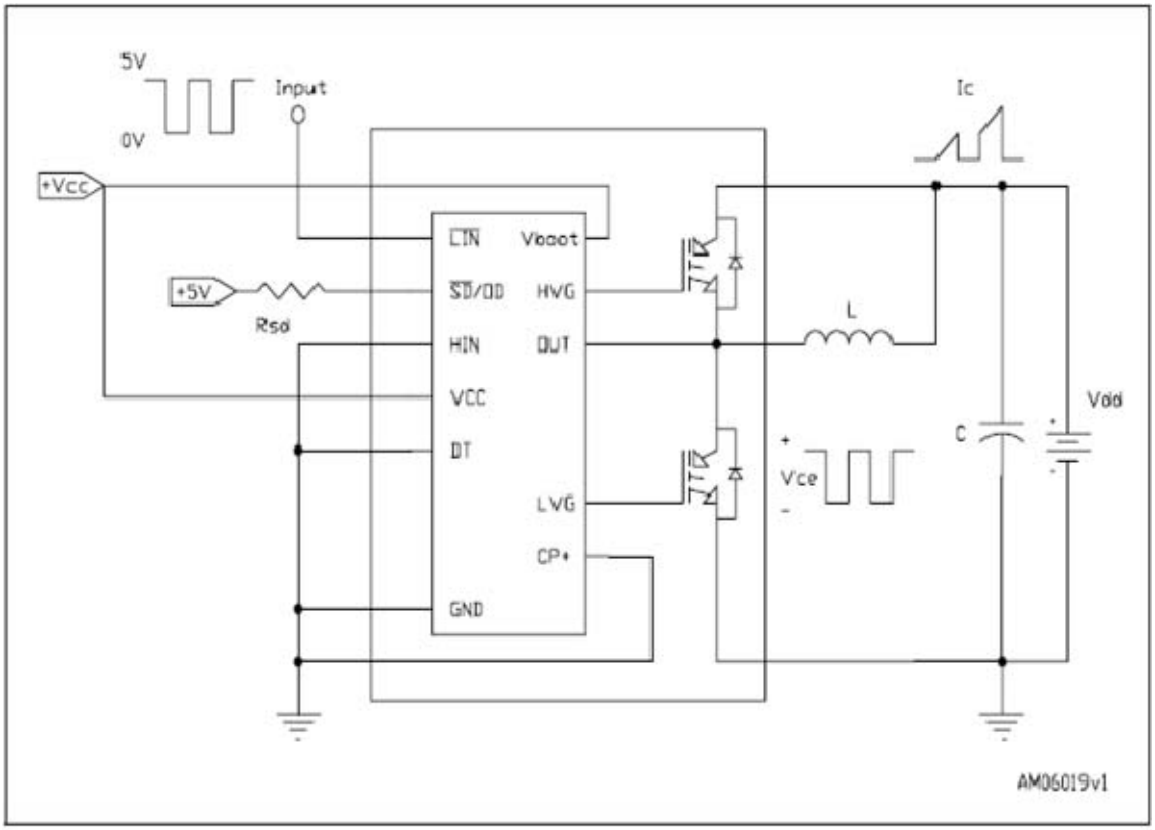


Figure 23. Test circuit switching time.

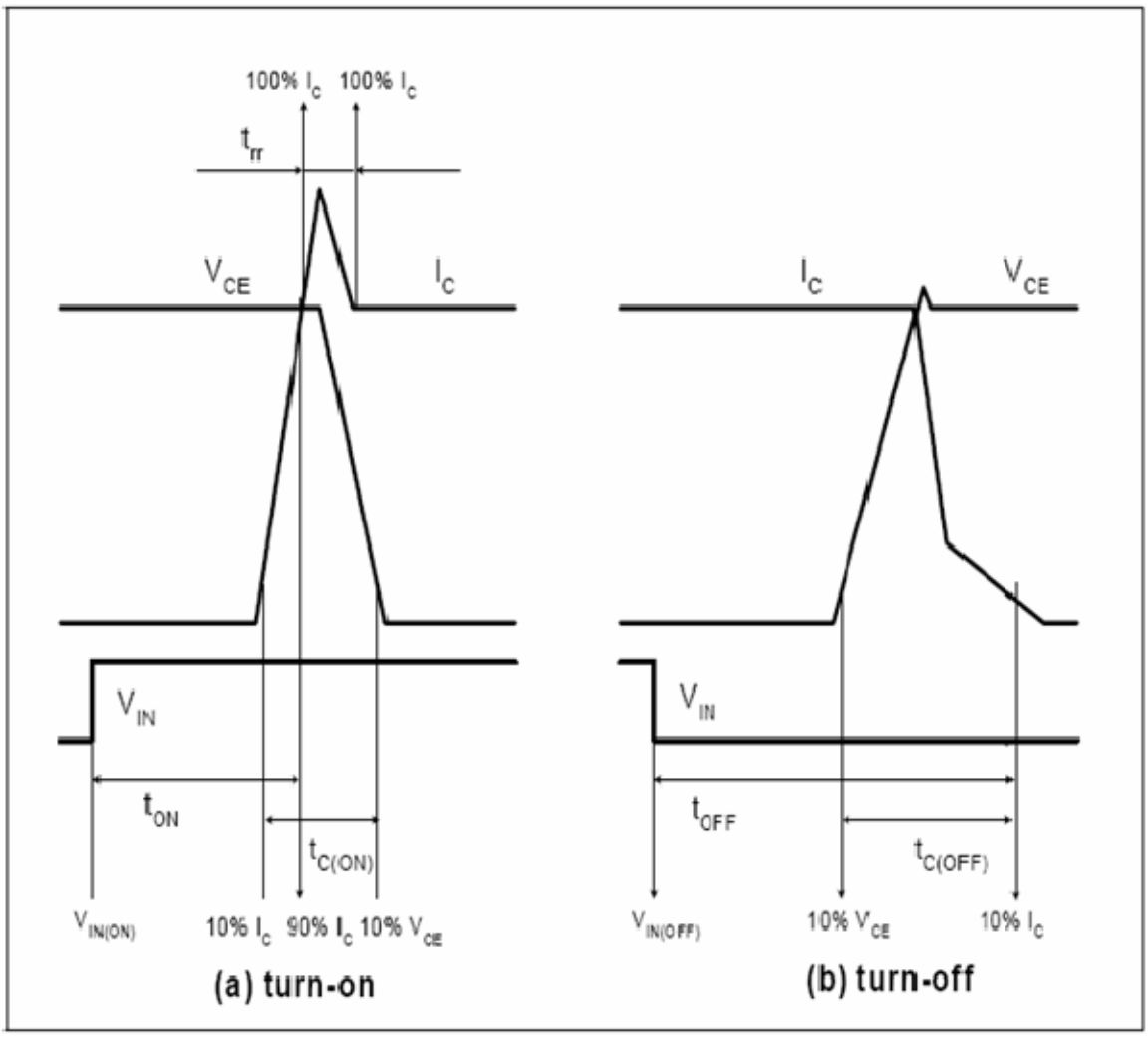


Figure 24. Switching time definition.

National Semiconductor

December 1994

LM35/LM35A/LM35C/LM35CA/LM35D Precision Centigrade Temperature Sensors

General Description

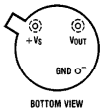
The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-202 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 μA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Connection Diagrams

TO-46
Metal Can Package*



TL/H/5516–1

*Case is connected to negative pin (GND)

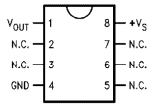
Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

TO-92
Plastic Package

TL/H/5516–2

Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

SO-8
Small Outline Molded Package

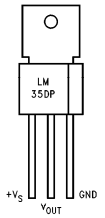


TL/H/5516–21

Top View
N.C. = No Connection

Order Number LM35DM
See NS Package Number M08A

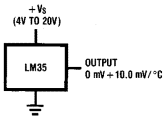
TO-202
Plastic Package



TL/H/5516–24

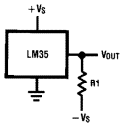
Order Number LM35DP
See NS Package Number P03A

Typical Applications



TL/H/5516–3

FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)



TL/H/5516–4

Choose $R_1 = -V_S/50\ \mu A$

V_{OUT} = +1,500 mV at +150°C
= +250 mV at +25°C
= −550 mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

RRD-B30M75/Printed in U. S. A.

Figure 25. LM35/LM35A/LM35C/LM35CA/LM35D precision centigrade temperature sensors (From: [10]).

LEM

Current Transducer LAH 25-NP

I_{PN} = 8-12-25 A

For the electronic measurement of currents: DC, AC, pulsed ..., with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

16038

Electrical data

I_{PN}	Primary nominal current rms				25		At
I_{PM}	Primary current, measuring range [1]				0 .. 55		At
R_M	Measuring resistance @ [2]		T_A = 70°C		T_A = 85°C		
			$R_{M\,min}$	$R_{M\,max}$	$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ I_{PN} [± At_{DC}]	0	284	0	280	Ω
		@ I_{PN} [At_{RMS}] [3]	0	182	0	178	Ω
	with ± 15 V	@ I_{PN} [± At_{DC}]	67	398	70	394	Ω
		@ I_{PN} [At_{RMS}] [3]	67	263	70	259	Ω
		@ I_P < I_{PN} [4]					
I_{SN}	Secondary nominal current rms				25		mA
K_N	Conversion ratio				1 - 2 - 3 : 1000		
V_C	Supply voltage (± 5 %)				± 12 .. 15		V
I_C	Current consumption				10 (@ ± 15V) + I_S		mA

Accuracy - Dynamic performance data

X	Accuracy [5] @ I_{PN}, T_A = 25°C		± 0.3		%
ε_L	Linearity error		< 0.2		%
			Typ	Max	
I_O	Offset current @ T_A = 25°C			± 0.15	mA
I_{OM}	Magnetic offset current @ I_P = 0 and specified R_M, after an overload of 5 x I_{PN}		± 0.20	± 0.25	mA
I_{OT}	Temperature variation of I_O	0°C .. + 70°C	± 0.10	± 0.60	mA
		- 25°C .. + 85°C	± 0.10	± 0.70	mA
$t_{r\,\varepsilon}$	Reaction time @ 10 % of I_{PN}		< 200		ns
t_r	Response time [6] to 90 % of I_{PN} step		< 500		ns
di/dt	di/dt accurately followed		> 200		A/µs
BW	Frequency bandwidth (- 1 dB)		DC .. 200		kHz

General data

T_A	Ambient operating temperature		- 25 .. + 85	°C
T_S	Ambient storage temperature		- 40 .. + 90	°C
R_S	Secondary coil resistance	@ T_A = 70°C	72	Ω
		@ T_A = 85°C	76	Ω
m	Mass		20	g
	Standards		EN 50178: 1997	

Notes: [1] During 10 s, with $R_M \leq 109\ \Omega$ (V_C = ± 15 V)
[2] Calculation of $R_{M\,min}$ with the maxi. power of the transistors = 0.307W @ 70°C and the maxi. power of the transistors = 0.302W @ 85°C
[3] 50 Hz Sinusoidal
[4] The measuring resistance $R_{M\,min}$ may be lower (see "LAH Technical Information" leaflet)
[5] Without I_S & I_{OM}
[6] With a di/dt of 100 A/µs.

Features

- Closed loop (compensated) multi-range current transducer using the Hall effect
- Printed circuit board mounting
- Insulated plastic case recognized according to UL 94-V0.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

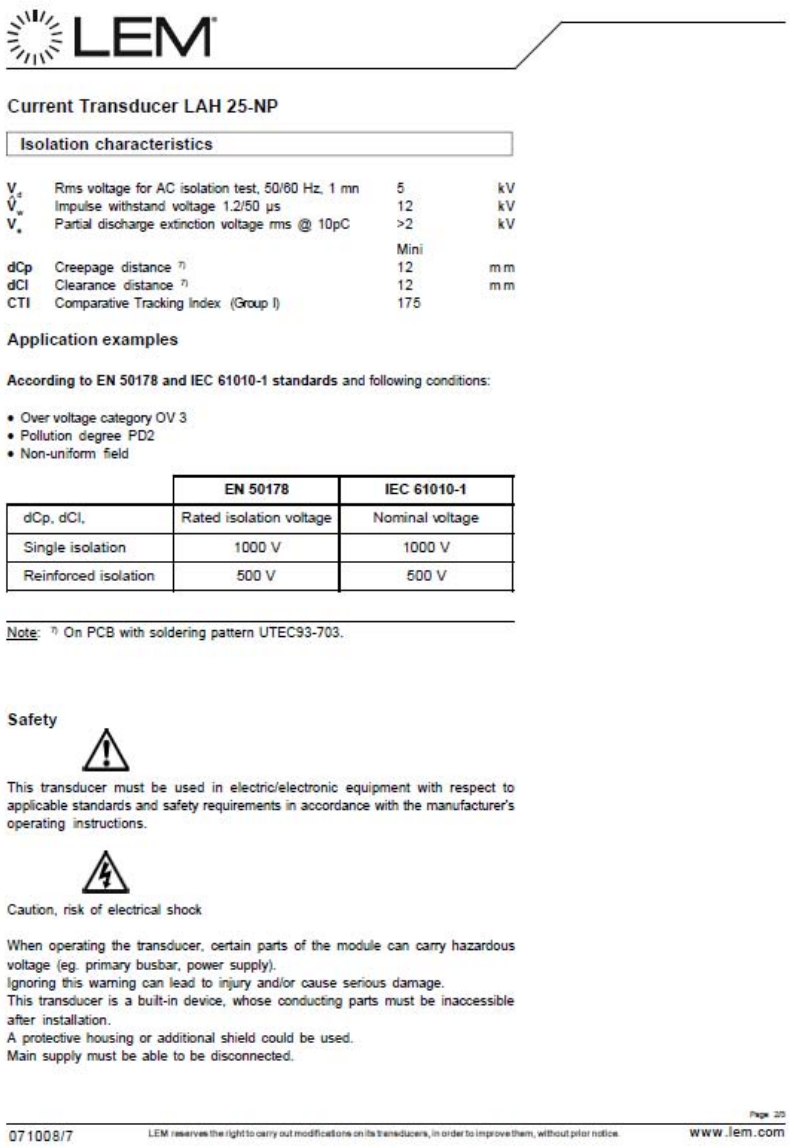
Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Application domain

- Industrial.

Figure 26. Current transducer LAH 25-NP data (From: [11]).



LEM

Current Transducer LAH 25-NP

Isolation characteristics

V_d	Rms voltage for AC isolation test, 50/60 Hz, 1 mn	5	kV
$\hat{V}_w$	Impulse withstand voltage 1.2/50 µs	12	kV
V_e	Partial discharge extinction voltage rms @ 10pC	>2	kV
		Mini	
dCp	Creepage distance 7)	12	mm
dCl	Clearance distance 7)	12	mm
CTI	Comparative Tracking Index (Group I)	175	

Application examples

According to EN 50178 and IEC 61010-1 standards and following conditions:

- Over voltage category OV 3
- Pollution degree PD2
- Non-uniform field

	EN 50178	IEC 61010-1
dCp, dCl,	Rated isolation voltage	Nominal voltage
Single isolation	1000 V	1000 V
Reinforced isolation	500 V	500 V

Note: 7) On PCB with soldering pattern UTEC93-703.

Safety

This transducer must be used in electric/electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.

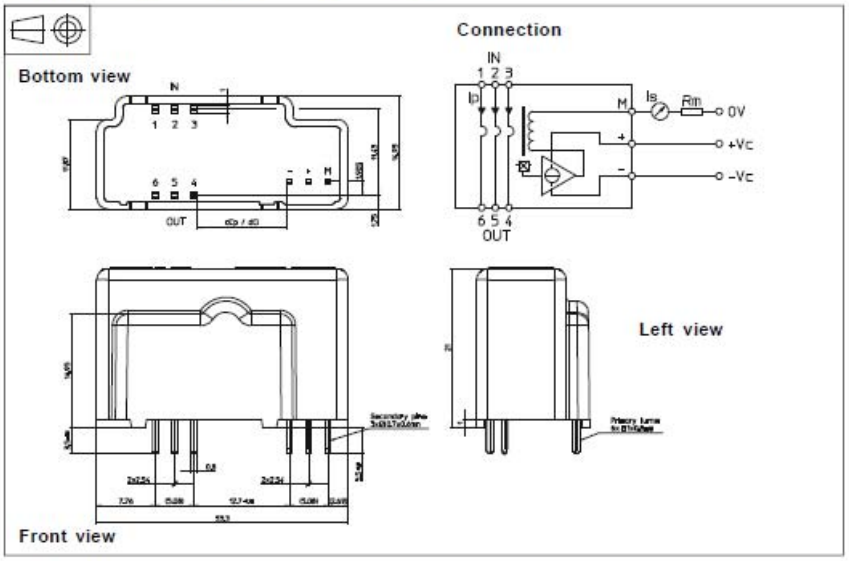
Caution, risk of electrical shock

When operating the transducer, certain parts of the module can carry hazardous voltage (eg. primary busbar, power supply).
Ignoring this warning can lead to injury and/or cause serious damage.
This transducer is a built-in device, whose conducting parts must be inaccessible after installation.
A protective housing or additional shield could be used.
Main supply must be able to be disconnected.

Figure 27. Current transducer LAH 25-NP characteristics (From: [11]).

LEM

Dimensions LAH 25-NP (in mm. 1 mm = 0.0394 inch)



Number of primary turns	Primary current nominal I_{PN} [A]	Primary current maximum I_P [A]	Nominal output current I_{SN} [mA]	Turns ratio K_N	Primary resistance R_P [mΩ]	Primary insertion Inductance L_P [µH]	Recommended PCB connections
1	25	55	25	1 : 1000	0.18	0.012	3 2 1 IN / OUT 4 5 6
2	12	27	24	2 : 1000	0.81	0.054	3 2 1 IN / OUT 4 5 6
3	8	18	24	3 : 1000	1.62	0.110	3 2 1 IN / OUT 4 5 6

Mechanical characteristics

- General tolerance ± 0.2 mm
- Fastening & connection of primary 6 pins 1 x 0.8 mm
  Recommended PCB hole 1.5 mm
- Fastening & connection of secondary 3 pins 0.7 x 0.6 mm
  Recommended PCB hole 1.2 mm

Remarks

- I_S is positive when I_P flows from terminals 1, 2, 3 (IN) to terminals 6, 5, 4 (OUT).
- The jumper temperature and PCB should not exceed 100°C.
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

Figure 28. Dimensions of LAH 25-NP (From: [11]).

FAIRCHILD SEMICONDUCTOR®

December 2009

FOD2200
Low Input Current Logic Gate Optocouplers

Features

- 1kV/μs minimum common mode rejection
- Compatible with LSTTL, TTL, and CMOS logic
- Wide V_{CC} range (4.5V to 20V)
- 2.5Mbd guaranteed over temperature
- Low input current (1.6mA)
- Three state output (no pullup resistor required)
- Guaranteed performance from 0°C to 85°C
- Hysteresis
- Safety approvals – UL, CSA, VDE (pending)
- V_{ISO} = 5kVRMS

Applications

- Isolation of high speed logic systems
- Computer peripheral interfaces
- Microprocessor system interfaces
- Ground loop elimination
- Pulse transformer replacement
- Isolated bus driver
- High speed line receiver

Description

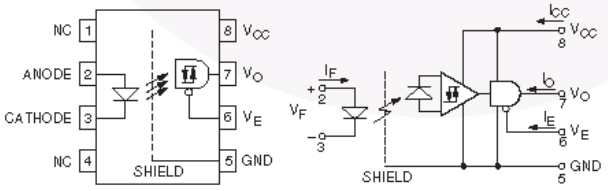
The FOD2200 is an optically coupled logic gate that combine an AlGaAs LED and an integrated high gain photo detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

The Electrical and Switching Characteristics of the FOD2200 are guaranteed over the temperature range of 0°C to 85°C and a V_{CC} range of 4.5V to 20V. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed opto-couplers. Logic signals are transmitted with a maximum propagation delay of 300ns. The FOD2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Truth Table (Positive Logic)

LED	Enable	Output
On	H	Z
Off	H	Z
On	L	H
Off	L	L

Functional Block Diagram and Schematic



Package Outlines

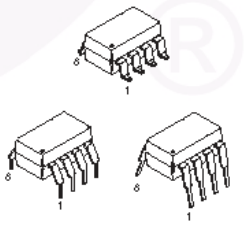


Figure 29. FOD2200 low input current logic gate optocouplers (From: [12]).

APPENDIX B. MATLAB CODE FOR VSI CHIPSCOPE SIMULATION

```
% Alex Julian, Giovanna Oriti, 13 Nov 2009
% acquiring 32 channels of data "totalpoints" times
buff_size=2^5*4;
if not(libisloaded('ftd2xx')) %if the library is NOT loaded
execute the following code
  loadlibrary('ftd2xx.dll', 'ftd2xxM.h');
end
h=libpointer('uint32Ptr', uint32(0));

disp('opening');
s=calllib('ftd2xx', 'FT_Open', 0, h);
if (s ~= 0)
  disp('open error');
  return;
end

% writing one word
dwBytesWritten=0;
pdwBytesWritten=libpointer('uint32Ptr', dwBytesWritten);
dwWxSize=1;
pdwWxSize=libpointer('uint32Ptr', dwWxSize);
tempy=uint8(0);         %sends zero,zero to input bits
ppcBufWrite=libpointer('uint32Ptr', tempy);

tempy=0;
ppcBufWrite.Value=tempy;
s=calllib('ftd2xx',      'FT_Write',      h,      ppcBufWrite,
pdwWxSize.Value, pdwBytesWritten);
tempy=2^7;   % sends 10 to input bits, loads data in RAM
ppcBufWrite.Value=tempy;
s=calllib('ftd2xx',      'FT_Write',      h,      ppcBufWrite,
pdwWxSize.Value, pdwBytesWritten);
pause(.1);

run_it=0;
tic;
flagit=0;
tempx=0;
dwBytesRead=0;          pdwBytesRead=libpointer('uint32Ptr',
dwBytesRead);
dwRxSize=0;               pdwRxSize=libpointer('uint32Ptr',
dwRxSize);
```

```
ok_flag=1;
totalpoints=2^11/4;
nopoints=0;
while (nopoints<totalpoints) & (ok_flag==1)
  nopoints=nopoints+1
  tempy=0;
  ppcBufWrite.Value=tempy;
  s=calllib('ftd2xx',     'FT_Write',     h,     ppcBufWrite,
pdwWxSize.Value, pdwBytesWritten);
  tempy=2^7+2^6;   % sends 11 to input bits
  ppcBufWrite.Value=tempy;
  s=calllib('ftd2xx',     'FT_Write',     h,     ppcBufWrite,
pdwWxSize.Value, pdwBytesWritten);
  flag=1;
  prev=0;
  pause(.04);
  s=calllib('ftd2xx', 'FT_GetQueueStatus', h, pdwRxSize);

  if (pdwRxSize.Value == 0)
    pause(.1);
    flagit=flagit+1;
    disp('closing');
    s=calllib('ftd2xx', 'FT_Close', h);
    libisloaded('ftd2xx');
    pause(.1);
    if  not(libisloaded('ftd2xx'))  %if  the  library  is  NOT
loaded execute the following code
      loadlibrary('ftd2xx.dll', 'ftd2xxM.h');
    end
    disp('opening');
    s=calllib('ftd2xx', 'FT_Open', 0, h);
    if (s ~= 0)
      disp('open error');
      return;
    end
    tempy=0;
    ppcBufWrite.Value=tempy;
    s=calllib('ftd2xx',    'FT_Write',    h,    ppcBufWrite,
pdwWxSize.Value, pdwBytesWritten);
    tempy=192;
    ppcBufWrite.Value=tempy;
    s=calllib('ftd2xx',    'FT_Write',    h,    ppcBufWrite,
pdwWxSize.Value, pdwBytesWritten);
  end
  while ((pdwRxSize.Value < buff_size) && s == 0)
    tempx=tempx+1
```

```
    s=calllib('ftd2xx', 'FT_GetQueueStatus', h, pdwRxSize);
    if ((pdwRxSize.Value ~= prev) && flag)
      flag=0;
    end
    prev=pdwRxSize.Value
  end

  pdwRxSize.Value=buff_size;
  pcBufRead=uint8(75*ones(1, pdwRxSize.Value/4));
  ppcBufRead=libpointer('uint32Ptr', pcBufRead);
  [u,   pr,   data,   pt]=calllib('ftd2xx',   'FT_Read',   h,
ppcBufRead, pdwRxSize.Value, pdwBytesRead);
  if (s~=0)
    disp('read error');
    ok_flag=0;
    return;
  end
  datamod=typecast(uint32(data), 'uint8');
  z(nopoints,:)=datamod; %storing 32 channels twice in the
z matrix [totalpoints x 64]
end
toc

disp('closing');
s=calllib('ftd2xx', 'FT_Close', h);
libisloaded('ftd2xx');

%post-processing and plotting data
%processing channel 1 data
z_LSB1=z(:,1);
z_MSB1=z(:,2);
ch1_data= shiftb2 (z_LSB1, z_MSB1, totalpoints);
%processing channel 2 data
z_LSB2=z(:,3);
z_MSB2=z(:,4);
ch2_data= shiftb2alj (z_LSB2, z_MSB2, totalpoints);
I_1=((((ch2_data/2^8)-1))/1.6985-2.5)*20/.625;
%processing channel 3 data
z_LSB3=z(:,5);
z_MSB3=z(:,6);
ch3_data= shiftb2alj (z_LSB3, z_MSB3, totalpoints);
dc_voltage1=ch3_data*2*0.0011308;

%processing channel 4 data
gain1=1/(1/3000+1/200000)/(1/(1/3000+1/200000)+56000*2)*1.0
5;
```

```
z_LSB4a=z(:,7);
z_MSB4a=z(:,8);
z_LSB4b=z(:,7+32);
z_MSB4b=z(:,8+32);
z_LSB4c=z(:,7+32+32);
z_MSB4c=z(:,8+32+32);
z_LSB4d=z(:,7+32+32+32);
z_MSB4d=z(:,8+32+32+32);
z_LSB4e=z(:,7+16);
z_MSB4e=z(:,8+16);
z_LSB4f=z(:,7+32+16);
z_MSB4f=z(:,8+32+16);
z_LSB4g=z(:,7+32+32+16);
z_MSB4g=z(:,8+32+32+16);
z_LSB4h=z(:,7+32+32+32+16);
z_MSB4h=z(:,8+32+32+32+16);

for ii=1:totalpoints/2
  z_LSB4(8*ii-7) =z_LSB4a(ii);
  z_LSB4(8*ii-6) =z_LSB4e(ii);
  z_LSB4(8*ii-5) =z_LSB4b(ii);
  z_LSB4(8*ii-4) =z_LSB4f(ii);
  z_LSB4(8*ii-3) =z_LSB4c(ii);
  z_LSB4(8*ii-2) =z_LSB4g(ii);
  z_LSB4(8*ii-1) =z_LSB4d(ii);
  z_LSB4(8*ii)  =z_LSB4h(ii);
  z_MSB4(8*ii-7) =z_MSB4a(ii);
  z_MSB4(8*ii-6) =z_MSB4e(ii);
  z_MSB4(8*ii-5) =z_MSB4b(ii);
  z_MSB4(8*ii-4) =z_MSB4f(ii);
  z_MSB4(8*ii-3) =z_MSB4c(ii);
  z_MSB4(8*ii-2) =z_MSB4g(ii);
  z_MSB4(8*ii-1) =z_MSB4d(ii);
  z_MSB4(8*ii)  =z_MSB4h(ii);
end

ch4_data= shiftb2alj (z_LSB4, z_MSB4, totalpoints*4);
ch4_final=ch4_data/2^7/gain1;
%processing channel 5 data
z_LSB5a=z(:,9);
z_MSB5a=z(:,10);
z_LSB5b=z(:,9+32);
z_MSB5b=z(:,10+32);
z_LSB5c=z(:,9+32+32);
z_MSB5c=z(:,10+32+32);
z_LSB5d=z(:,9+32+32+32);
```

```
z_MSB5d=z(:,10+32+32+32);
z_LSB5e=z(:,9+16);
z_MSB5e=z(:,10+16);
z_LSB5f=z(:,9+32+16);
z_MSB5f=z(:,10+32+16);
z_LSB5g=z(:,9+32+32+16);
z_MSB5g=z(:,10+32+32+16);
z_LSB5h=z(:,9+32+32+32+16);
z_MSB5h=z(:,10+32+32+32+16);

for ii=1:totalpoints/2
  z_LSB5(8*ii-7) =z_LSB5a(ii);
  z_LSB5(8*ii-6) =z_LSB5e(ii);
  z_LSB5(8*ii-5) =z_LSB5b(ii);
  z_LSB5(8*ii-4) =z_LSB5f(ii);
  z_LSB5(8*ii-3) =z_LSB5c(ii);
  z_LSB5(8*ii-2) =z_LSB5g(ii);
  z_LSB5(8*ii-1) =z_LSB5d(ii);
  z_LSB5(8*ii)  =z_LSB5h(ii);
  z_MSB5(8*ii-7) =z_MSB5a(ii);
  z_MSB5(8*ii-6) =z_MSB5e(ii);
  z_MSB5(8*ii-5) =z_MSB5b(ii);
  z_MSB5(8*ii-4) =z_MSB5f(ii);
  z_MSB5(8*ii-3) =z_MSB5c(ii);
  z_MSB5(8*ii-2) =z_MSB5g(ii);
  z_MSB5(8*ii-1) =z_MSB5d(ii);
  z_MSB5(8*ii)  =z_MSB5h(ii);
end
ch5_data= shiftb2alj (z_LSB5, z_MSB5, totalpoints*4);
ch5_final=ch5_data/2^7/gain1;
%processing channel 6 data
gain2=1/(1/6800+1/200000)/(1/(1/6800+1/200000)+120000*2)*1.
05; %dc sensor gain
gainI=3/1000*330;      %current sensor gain
z_LSB6a=z(:,11);
z_MSB6a=z(:,12);
z_LSB6b=z(:,11+32);
z_MSB6b=z(:,12+32);
z_LSB6c=z(:,11+32+32);
z_MSB6c=z(:,12+32+32);
z_LSB6d=z(:,11+32+32+32);
z_MSB6d=z(:,12+32+32+32);
z_LSB6e=z(:,11+16);
z_MSB6e=z(:,12+16);
z_LSB6f=z(:,11+32+16);
z_MSB6f=z(:,12+32+16);
```

```
z_LSB6g=z(:,11+32+32+16);
z_MSB6g=z(:,12+32+32+16);
z_LSB6h=z(:,11+32+32+32+16);
z_MSB6h=z(:,12+32+32+32+16);

for ii=1:totalpoints/2
  z_LSB6(8*ii-7) =z_LSB6a(ii);
  z_LSB6(8*ii-6) =z_LSB6e(ii);
  z_LSB6(8*ii-5) =z_LSB6b(ii);
  z_LSB6(8*ii-4) =z_LSB6f(ii);
  z_LSB6(8*ii-3) =z_LSB6c(ii);
  z_LSB6(8*ii-2) =z_LSB6g(ii);
  z_LSB6(8*ii-1) =z_LSB6d(ii);
  z_LSB6(8*ii)  =z_LSB6h(ii);
  z_MSB6(8*ii-7) =z_MSB6a(ii);
  z_MSB6(8*ii-6) =z_MSB6e(ii);
  z_MSB6(8*ii-5) =z_MSB6b(ii);
  z_MSB6(8*ii-4) =z_MSB6f(ii);
  z_MSB6(8*ii-3) =z_MSB6c(ii);
  z_MSB6(8*ii-2) =z_MSB6g(ii);
  z_MSB6(8*ii-1) =z_MSB6d(ii);
  z_MSB6(8*ii)  =z_MSB6h(ii);
end
ch6_data= shiftb2alj (z_LSB6, z_MSB6, totalpoints*4);
ch6_final=ch6_data/2^8/gainI;
%processing channel 7 data
z_LSB7a=z(:,13);
z_MSB7a=z(:,14);
z_LSB7b=z(:,13+32);
z_MSB7b=z(:,14+32);
z_LSB7c=z(:,13+32+32);
z_MSB7c=z(:,14+32+32);
z_LSB7d=z(:,13+32+32+32);
z_MSB7d=z(:,14+32+32+32);
z_LSB7e=z(:,13+16);
z_MSB7e=z(:,14+16);
z_LSB7f=z(:,13+32+16);
z_MSB7f=z(:,14+32+16);
z_LSB7g=z(:,13+32+32+16);
z_MSB7g=z(:,14+32+32+16);
z_LSB7h=z(:,13+32+32+32+16);
z_MSB7h=z(:,14+32+32+32+16);

for ii=1:totalpoints/2
  z_LSB7(8*ii-7) =z_LSB7a(ii);
  z_LSB7(8*ii-6) =z_LSB7e(ii);
```

```
  z_LSB7(8*ii-5) =z_LSB7b(ii);
  z_LSB7(8*ii-4) =z_LSB7f(ii);
  z_LSB7(8*ii-3) =z_LSB7c(ii);
  z_LSB7(8*ii-2) =z_LSB7g(ii);
  z_LSB7(8*ii-1) =z_LSB7d(ii);
  z_LSB7(8*ii)  =z_LSB7h(ii);
  z_MSB7(8*ii-7) =z_MSB7a(ii);
  z_MSB7(8*ii-6) =z_MSB7e(ii);
  z_MSB7(8*ii-5) =z_MSB7b(ii);
  z_MSB7(8*ii-4) =z_MSB7f(ii);
  z_MSB7(8*ii-3) =z_MSB7c(ii);
  z_MSB7(8*ii-2) =z_MSB7g(ii);
  z_MSB7(8*ii-1) =z_MSB7d(ii);
  z_MSB7(8*ii)  =z_MSB7h(ii);
end
ch7_data= shiftb2alj (z_LSB7, z_MSB7, totalpoints*4);
ch7_final=ch7_data/2^8/gainI;

%processing channel 15 and 16 data to create time vector
z_LSB15=z(:,29);
z_MSB15=z(:,30);
z_LSB16=z(:,31);
z_MSB16=z(:,32);
timedataold=   shift_time2   (z_LSB15,   z_MSB15,   z_LSB16,
z_MSB16, totalpoints);

timedata=[0:(2^11-1)]/25e6*2^9;

Figure(1);
plot(timedata,ch4_final,'b','linewidth',2);
hold on;
plot(timedata,ch5_final,'g','linewidth',2);
hold off;
title('channel 4 and 5 data')
grid;
Figure(2);
plot(timedata,ch7_final,'g','linewidth',2);
hold on;
plot(timedata,ch7_final,'go','linewidth',2);
hold off;
title('channel 7 data')
grid;
```

```
Figure(3);
plot(timedata,ch6_final,'b','linewidth',2);
title('channel 6 data')
grid;
```

MATLAB CODE FOR TEMPERATURE VS TIME SIMULATION

```
%%Temp Vs Time MEASUREMENTS

Time=[0,60,120,180,240,300,360,420,480,540,600,660,720,780,840 ];
Temp=[23,30.4,37,39.9,43.4,46,49,50.8,52.4,52.9,53,53,53,53,53];

plot(Time,Temp,'x')
hold on;
plot(Time,Temp,'r')
grid on;
title('Thermal Behavior analysis Data for LM35 on IPM IGBT Heat sink'),
xlabel('Time[s]'), ylabel('Temperature[C]');
```

Published with MATLAB®

MATLAB Code for Low Pass Filter Simulation

```
LowPASS Filter
R1=2*56e3;
R2=3e3;
C=4700e-12;
freq=[1:10000]*5;
jw=j*2*pi*freq;
Zp=R2.*(1./jw./C)./(R2+(1./jw./C));
gain=Zp./(R1+Zp);
Figure(1);
semilogx(freq,20*log10(abs(gain)));
grid;
title('Lowpass filter Amplitude Response'), xlabel ('Frequency(Hz)'),
ylabel('Decibel')
Figure(2);
semilogx(freq,angle(gain)*180/pi);
grid;
title('Lowpass filter Phase shift'), xlabel ('Frequency(Hz)'),
ylabel('Phase(degrees)')
```

APPENDIX C. SEMITEACH® POWER INVERTER

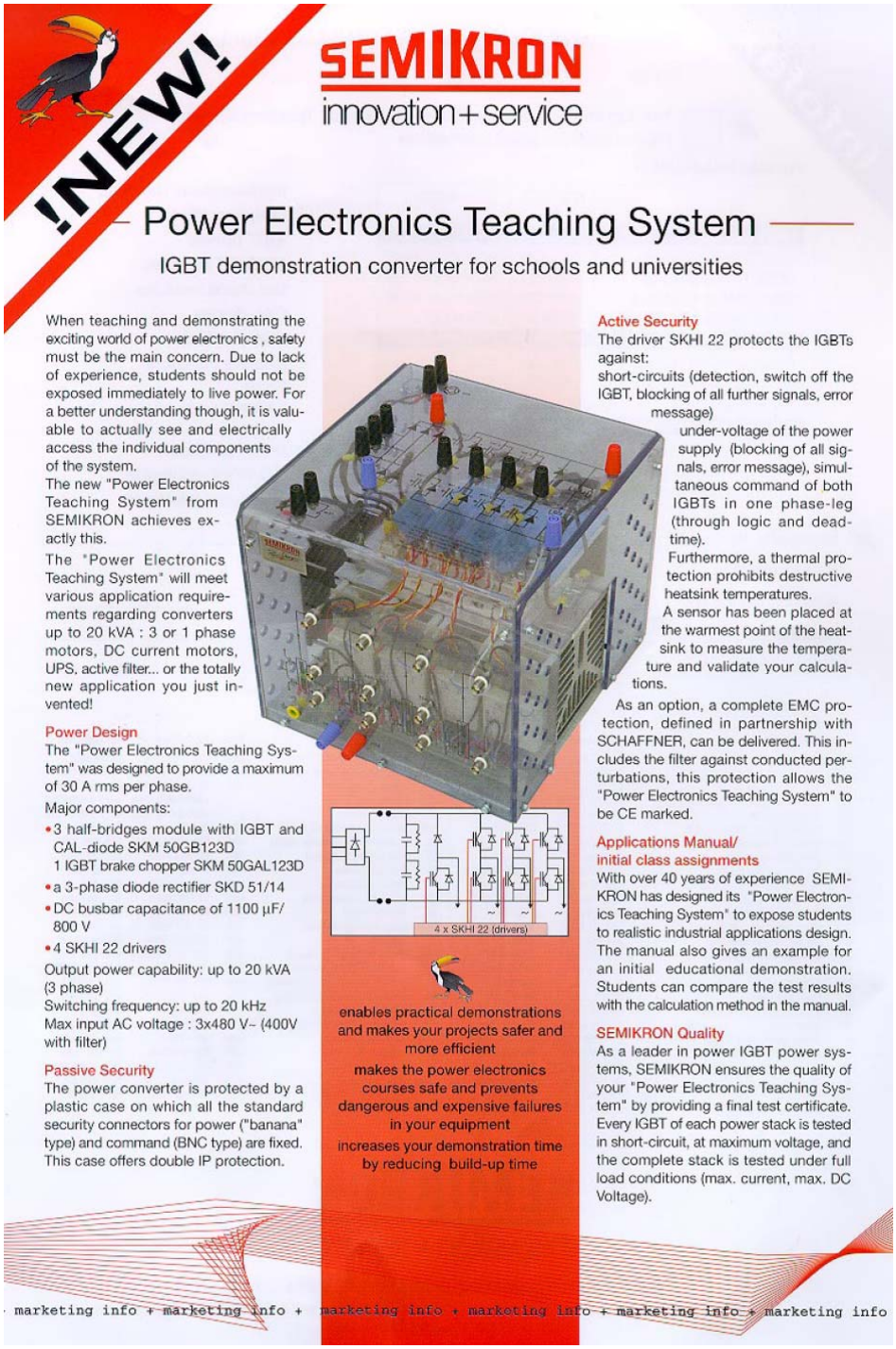


Figure 30. SEMITEACH® power inverter (From: [13])

THIS PAGE INTENTIONALLY LEFT BLANK

LIST OF REFERENCES

[1] E. O'Connor, "Field programmable gate array control of power systems in graduate student laboratories," M.S. thesis, Naval Postgraduate School, Monterey, California, 2006.

[2] A research and development of next generation Naval Integrated Power Systems (IPS), Broad Agency Announcement (BAA) Research Opportunity Description Paper, Department of the Navy, NAV SEA SYSTEM COMMAND, NAVSEA HQ, Navy Yard, Washington, DC, March 2010.

[3] ST product datasheets STGIPS20K60 IGBT intelligent Power Module (IPM), July 2010, http://www.st.com.

[4] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics*, 3rd Edition. Hoboken, New Jersey: John Wiley and Sons, Inc., 2003.

[5] Frank Filler, "A pulsed power system design using lithium –ion batteries and one charger per battery," M.S. thesis, Naval Postgraduate School, Monterey, California, December 2009.

[6] NEW_ANALOG_BOARD4REV1.EPC schematic developed by Professor Alexander L. Julian, August 2010.

[7] MEMEC™ corporation technical staff, *Virtex-4™ LC Development Board User's Guide Version 2.0*, MEMEC™ Corporation, 2005.

[8] XILINX® Products and Services, "Basic FPGA architecture and ChipScope™ Pro," April 2007, http://www.xilinx.com/univ/downld_partnerteaching.htm; http://www.xilinx.com/ise/optional_prod/cspro.htm.

[9] A. Adaman, *Voltage Regulator Handbook by Linear Design Engineering*, Fairchild Camera and Instrument Cooperation, 1987.

[10] National Semiconductors datasheets LM35 precision centigrade temperature sensors, December 1994, National Semiconductors Corporation.

[11] LEM products datasheets current transducer LAH_25-NP, October 2008, http://www.lem.com.

[12] Fairchild Semiconductors datasheets low input current logic gate optocouplers, December 2009, http://www.fairchildsemi.com.

[13] Semikron® Products Marketing Information, "Power electronics systems (SEMISTACK)," April 2007, http://www.semikron.com/internet/index.jsp?sekId=361.

[14] Mathworks Product Marketing Information, "Simulink®-simulation and model-based design," April 2007, http://www.mathworks.com/products/simulink/?BB=1.

[15] "EC3150 Laboratory 1: Power electronics lab tools familiarization," class notes for EC3150, Department of Electrical and Computer Engineering, Naval Postgraduate School, Summer 2007.

[16] J. Lund, “Field programmable gate array hysteresis control of parallel connected inverters,” M.S. thesis, Naval Postgraduate School, Monterey, California, 2006.

[17] Analogdevices.com, *AD7864 Specifications*, 2007.

[18] P. Krause, O. Wasynczuk, and S. Sodhoff, *Analysis of Electric Machinery and Drive Systems*, 2nd Edition. New York: IEEE Press, 2002.

INITIAL DISTRIBUTION LIST

1. Defense Technical Information Center
   Ft. Belvoir, Virginia

2. Dudley Knox Library
   Naval Postgraduate School
   Monterey, California

3. Dr. R. Clark Robertson
   Electrical Engineering and Computer Department
   Code EC
   Naval Postgraduate School
   Monterey, California

4. Dr. Alexander Julian
   Electrical Engineering and Computer Department
   Code EC
   Naval Postgraduate School
   Monterey, California

5. Dr. Roberto Cristi
   Electrical Engineering and Computer Department
   Code EC
   Naval Postgraduate School
   Monterey, California

6. LT Henry O. Amadasu
   United States Navy
   Monterey, California